Cyntec Power Module Solutions for FPGA

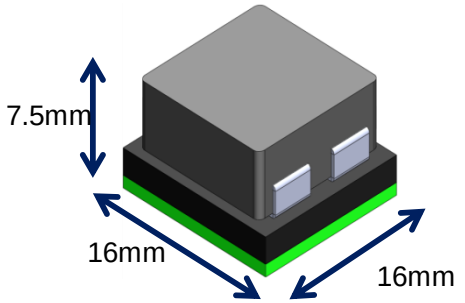
MSN12AD60-RUD

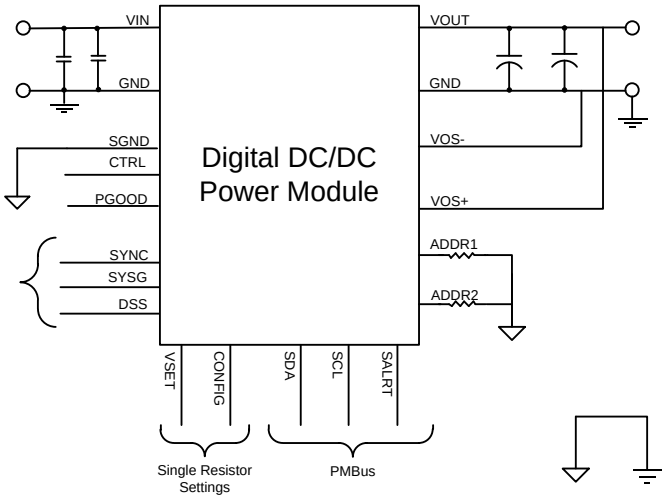
Cyntec Co., Ltd.

MSN12AD60-RUD FEATURE & APPLICATION

FEATURES:

- Maximum Load:60A
- Input Voltage Range from 8V to 15V
- Output Voltage Range from 0.6V to 1.8V
- Configurable Digital Loop Compensation
  - Auto-Control Real-Time Adaptive Loop Compensation
- SMBus Interface with PMBus Power System Management Protocol
- Precision Measurement & Telemetry Reporting: VOUT, IOUT, VIN, EOUT, Temperature, Fsw, Duty Cycle
- Programmable Protection & Warning
  - Output OVP, OCP,SCP, UV, LOS Warning
  - Input UVLO, OVLO
  - Internal & External OTP
  - Phase Loss fault
  - Temperature Compensated Faults
  - Configurable SALRT
- Single-Pin Configuration with Eight Profile Tables
- Power Management and Conversion
  - SwitchFrequencyto500kHz
  - Programmable VOUT, Voltage Tracking, Margining, & Sequencing
  - Adjustable Load-Line
  - Power Good, System Good, & Remote Power Down
- 16mmX16mmX7.5mm (Typical) BGA Package





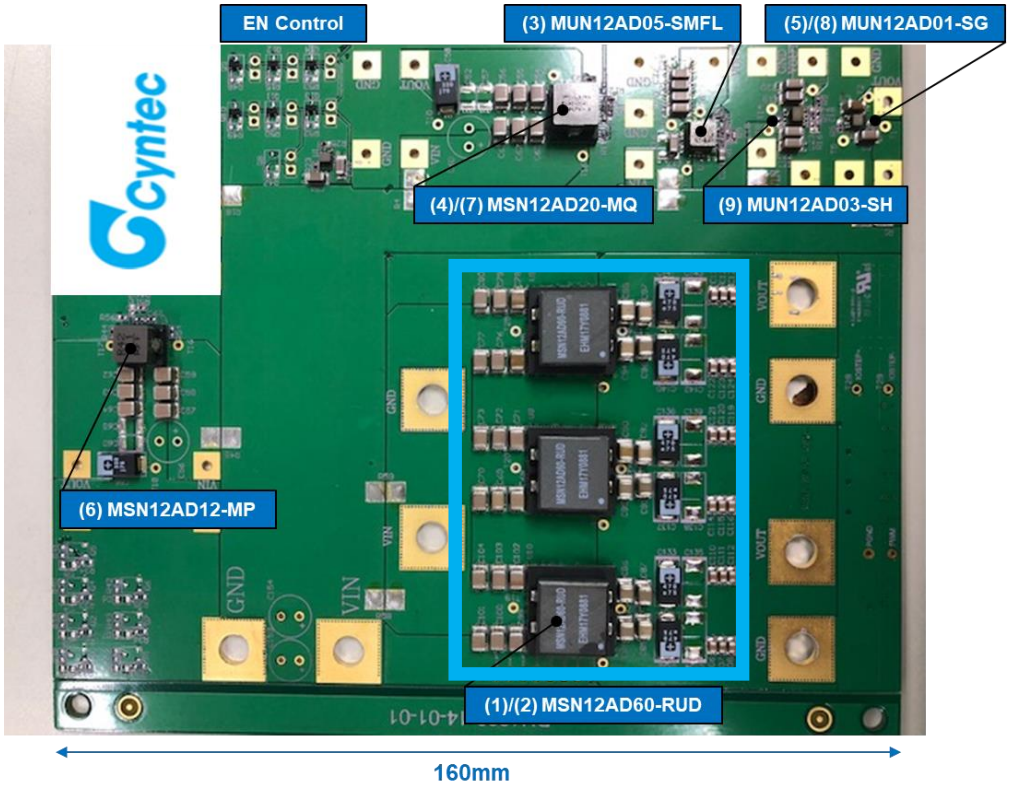
APPLICATIONS:

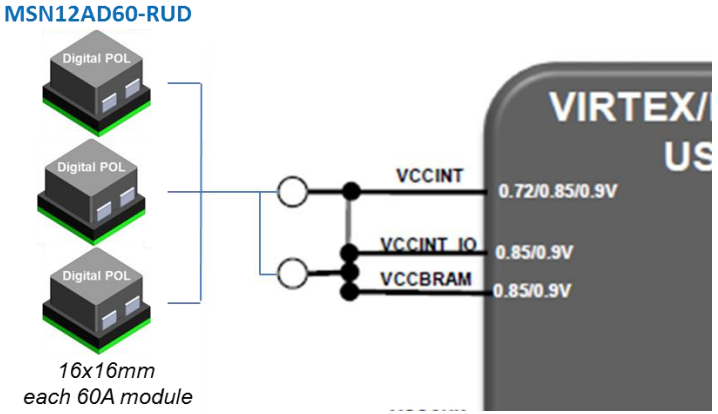
- VDDQ for DDR Memory; Supports Over-Clocking Applications
- ASIC, FPGA, Microprocessor, Memory
- Networking, Communications, Storage, Server, Computing
- Advanced Power Modules & General Purpose POL

MSN12AD60-RUD for Xilinx XCVU13P

Specifications

- Assuming **VCCINT/VCCINT_IO/VCCBRAM** have the same voltage, say 0.85V
- Max. current 145A (120A for INT, 25A for IO/BRAM)
- Transient response: ±3%, 25% step, 100A/us
- Decoupling capacitance 8x480uF/ 10x100uF/ 20x4.7uF





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MSN12AD60-RUD for Xilinx XCVU13P Efficiency

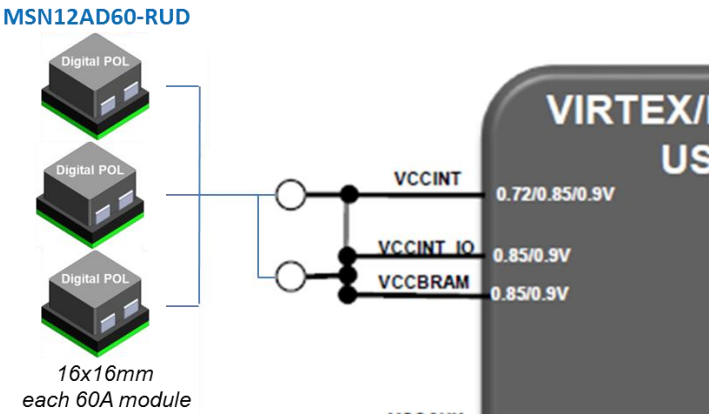
Test Condition

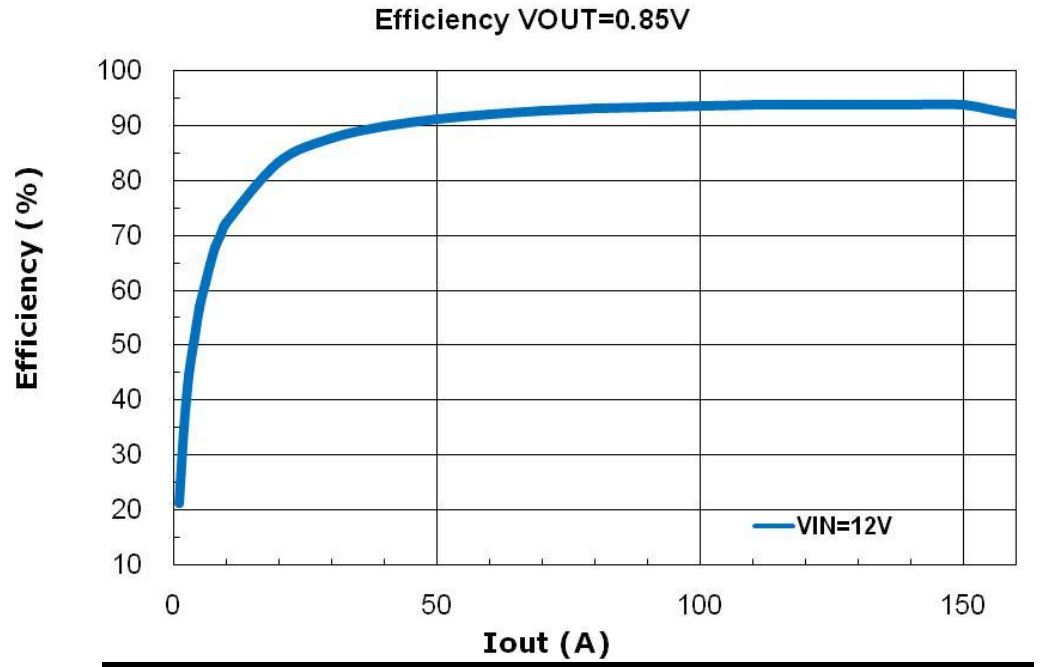
VIN=12V VOUT=0.85V IOUT=180A

Module: Cyntec MSN12AD60-RUD X 3 pcs

Input Capacitor: 22uF x 18pcs

Output Capacitor: 480uF x 8 / 100uF x 10pcs / 4.7uF x 20 pcs





VOUT=0.85V Pk-Pk Efficiency= 93% for IOUT=100A

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MSN12AD60-RUD for Xilinx XCVU13P
Ripple

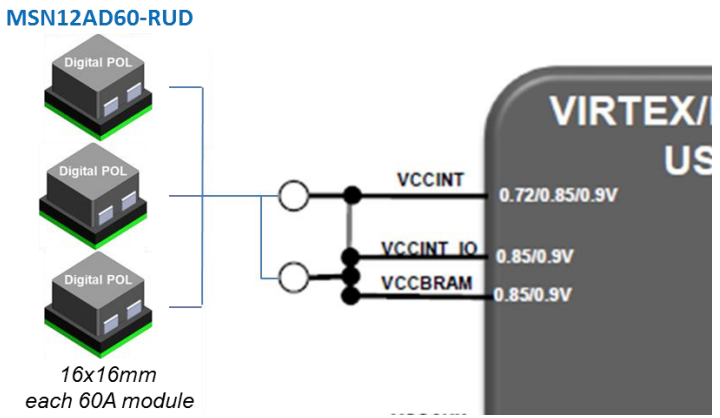
Test Condition

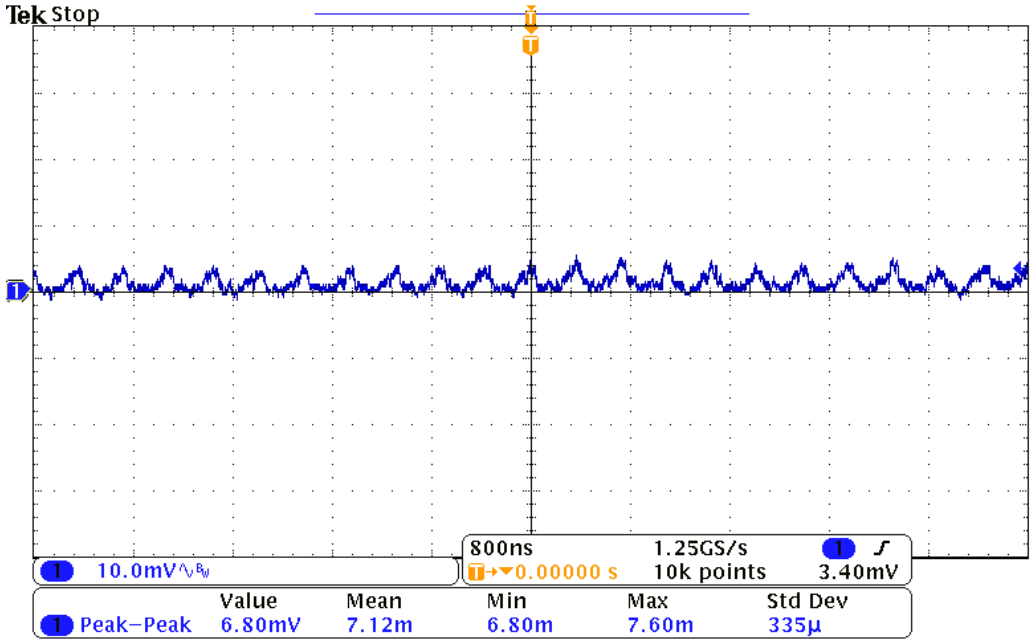
VIN=12V VOUT=0.85V IOUT=180A

Module: Cyntec MSN12AD60-RUD X 3 pcs

Input Capacitor: 22uF x 18pcs

Output Capacitor: 480uF x 8 / 100uF x 10pcs / 4.7uF x 20 pcs





VOUT=0.85V Pk-Pk 6.80mV for IOUT=180A

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MSN12AD60-RUD for Xilinx XCVU13P Transient

Test Condition

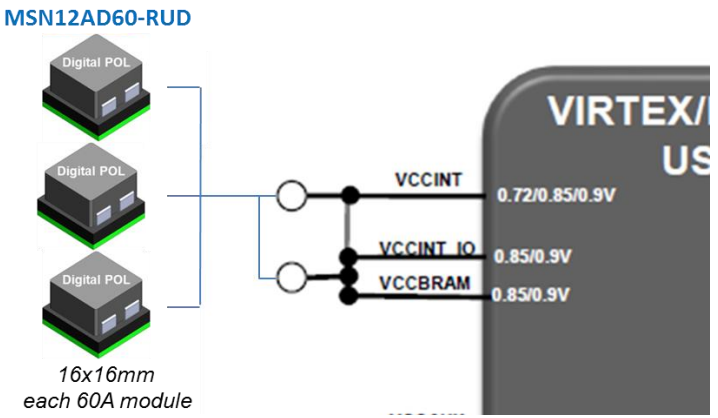
VIN=12V VOUT=0.85V IOUT=180A

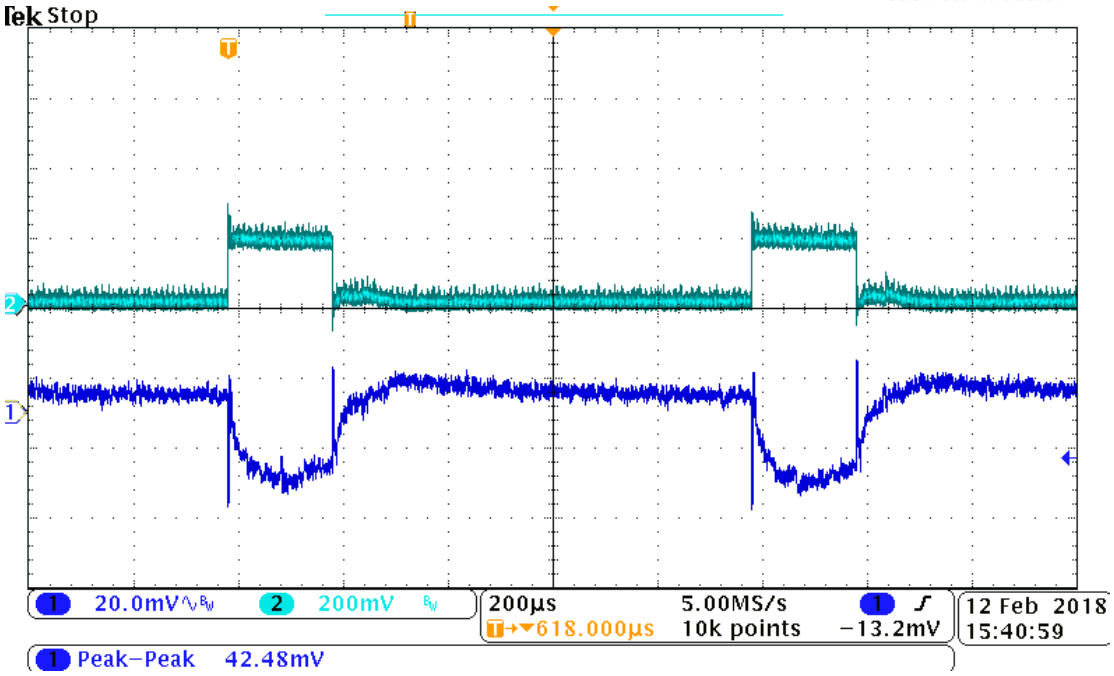
Module: Cyntec MSN12AD60-RUD X 3 pcs

Input Capacitor: 22uF x 18pcs

Output Capacitor: 480uF x 8 / 100uF x 10pcs / 4.7uF x 20 pcs

Transient < ± 3%, >25% step (0-40A), 100A/us





VOUT=0.85V Pk-Pk Transient =42.48mV for IOUT=0~40A

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MSN12AD60-RUD for Xilinx XCVU13P Thermal

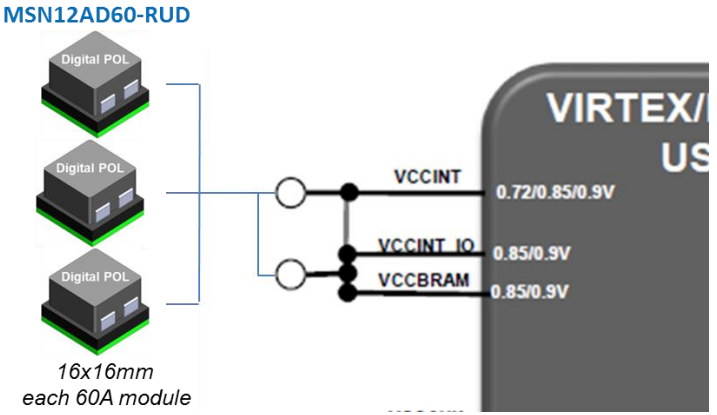
Test Condition

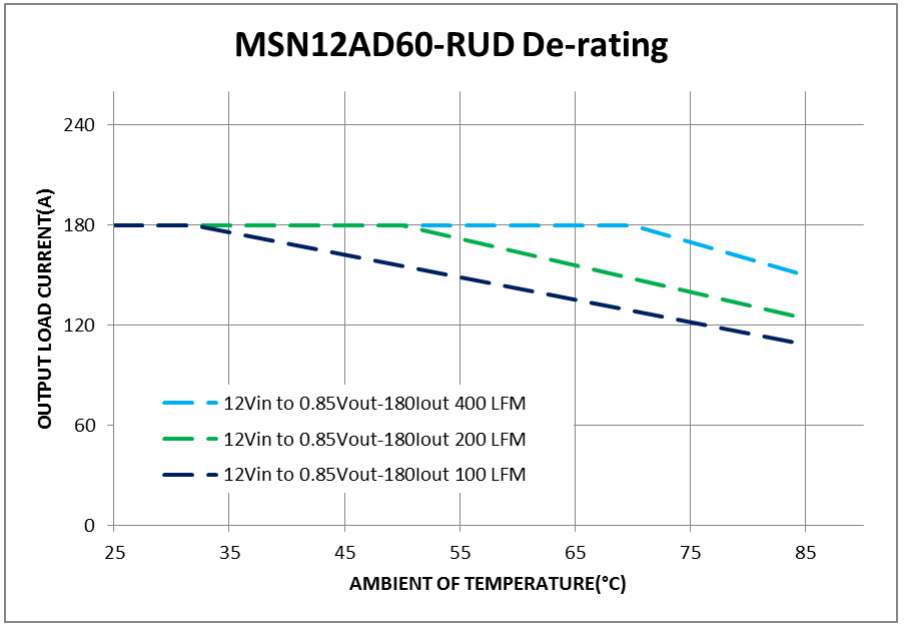
VIN=12V VOUT=0.85V IOUT=180A

Module: Cyntec MSN12AD60-RUD X 3 pcs

Input Capacitor: 22uF x 18pcs

Output Capacitor: 480uF x 8 / 100uF x 10pcs / 4.7uF x 20 pcs





200 LMF 50℃ De-rating

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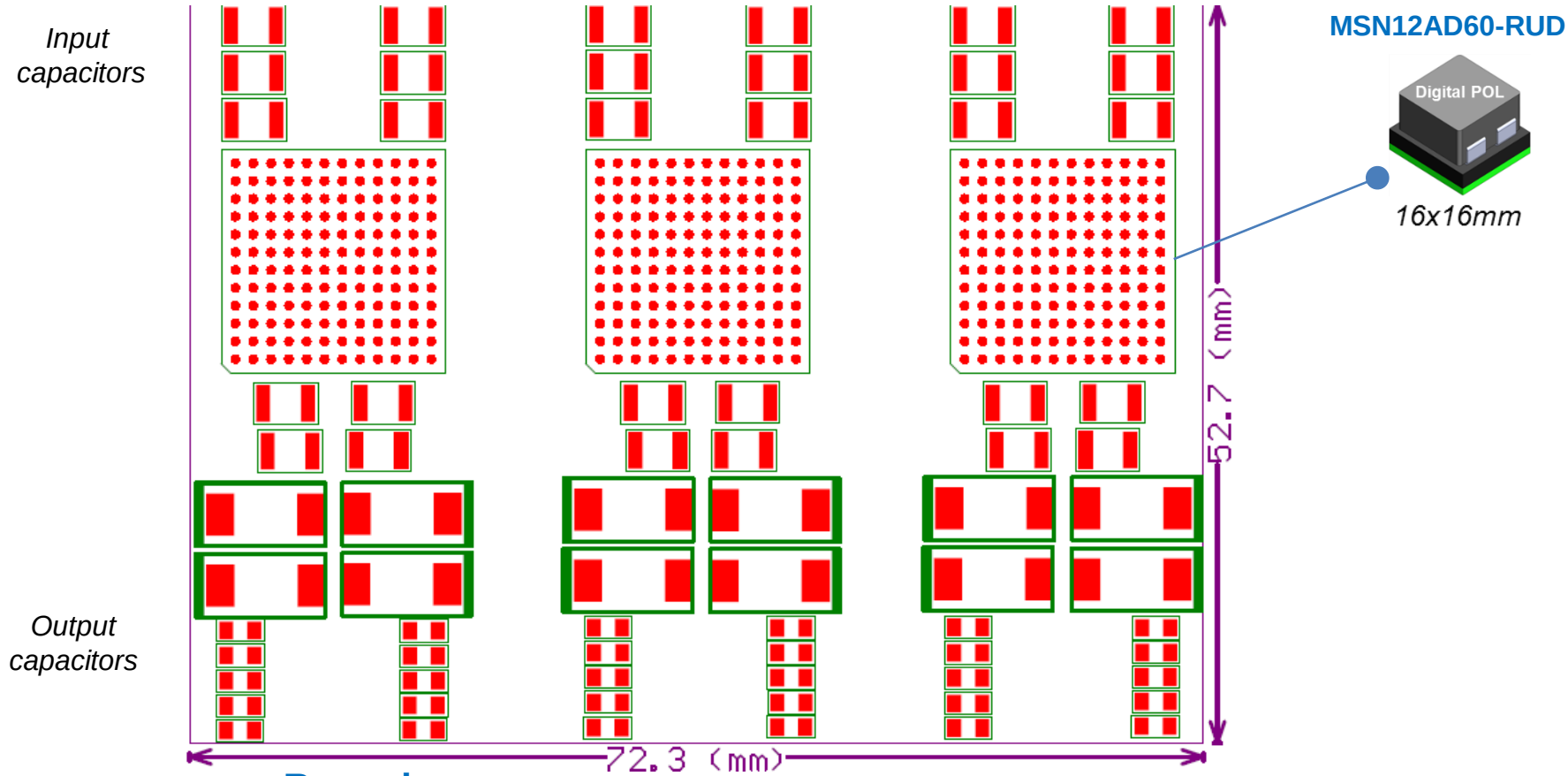
Layout Example of the 60A module

(Layout is for reference only --- single-sided SMT. Further optimization is possible in terms of output characteristics and actual application environment)



Remarks

- Input capacitance: 22uF x18pcs
- Output capacitance: 480uF x12pcs + 100uF x12pcs + 4.7uF x20pcs
- Arrangement could be optimized based on output transient requirements