uPOL Module

3A, High Efficiency uPOL Module

MUN24AD03-SM

FEATURES:

- High Density uPOL Module
- 3A Output Current
- Input Voltage Range from 4.5V to 34V
- Output Voltage Range from 3V to 12V
- 94% Peak Efficiency(@Vin=24V)
- Automatic Power Saving/PWM Mode
- Protections (OCP: Non-latching, OTP)
- Internal Soft Start
- Compact Size: 6mm*6mm*3.5mm(Max)
- Pb-free for RoHS compliant
- MSL 2, 250°C Reflow

APPLICATIONS:

- Distributed Power Supply
- Server, Workstation, and Storage

GENERAL DESCRIPTION:

The uPOL module is non-isolated DC-DC converters that can deliver up to 3A of output current. The PWM switching regulator, high frequency power inductor are integrated in one hybrid package. It only needs some passive component to use this uPOL module easily.

The module has automatic operation with PWM mode and power saving mode according to loading. Other features include remote enable function, internal soft-start, non-latching over current protection.

The low profile and compact size package (6.0mm × 6.0mm x 3.5mm) is suitable for automated assembly by standard surface mount equipment. The uPOL module is Pb-free and RoHS compliant.

TYPICAL APPLICATION CIRCUIT & PACKAGE SIZE:

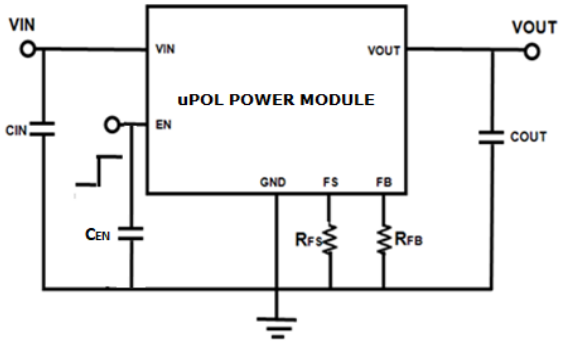


FIG.1 TYPICAL APPLICATION CIRCUIT

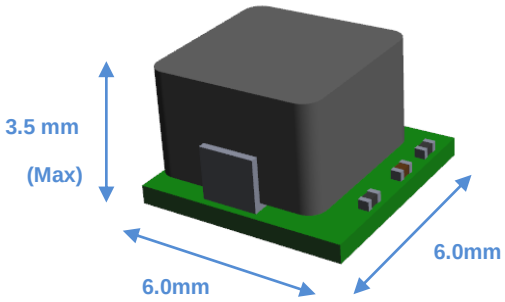


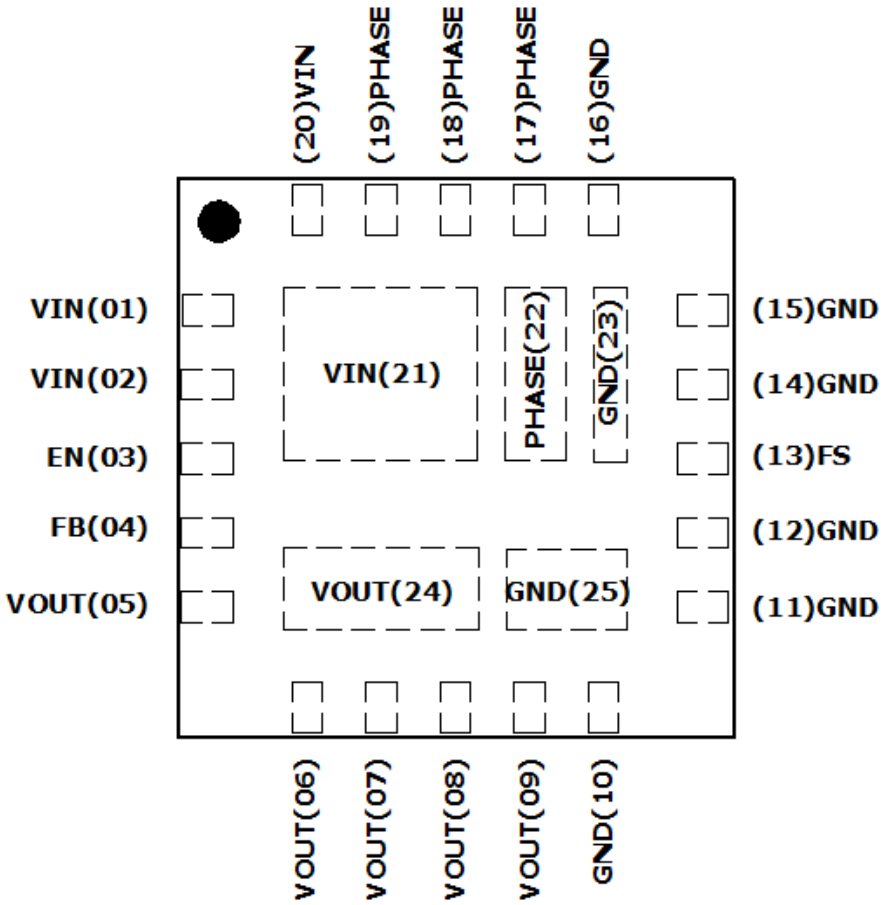
FIG.2 HIGH DENSITY POWER MODULE

ORDER INFORMATION:

Part Number	Ambient Temp. Range (°C)	Package (Pb-Free)	MSL	Note
MUN24AD03-SM	-40 ~ +85	QFN	Level 2	-

Order Code	Packing	Quantity
MUN24AD03-SM	Tape and reel	1000

PIN CONFIGURATION:



TOP VIEW

PIN DESCRIPTION:

Symbol	Pin No.	Description
VIN	1, 2, 20	Power input pin. Connect to the input rail and thermal exposed pad of VIN_TPD(21) for heat transferring. Place the ceramic type input capacitor as closely as possible to this pin. At least 10uF input capacitance is needed.
EN	3	On/Off control pin for module. Pull high to turn on. Pull low to turn off. Do not leave this pin floating.
FB	4	Feedback input. Connect an external resistor between FB and GND, refer to TABEL 1 output voltage setting.
VOUT	5, 6, 7, 8, 9	Power output pin. Connect to output and thermal exposed pad of VOUT_TPD(24) for heat transferring. Place the output capacitors as closely as possible to this pin. At least 22uF output capacitance is needed.
GND	10, 11, 12, 14, 15, 16	Power ground pin. Connect to thermal exposed pad of GND_TPD(23, 25) for heat transferring.
FS	13	Connect a 133kΩ resistor to ground to Setting 750KHz switching frequency.
PHASE	17, 18, 19	Phase Node. Connect to thermal exposed pad of PHASE_TPD(22) for heat transferring.
VIN_TPD	21	Power input pin. Connect to input rail. Used for heat transferring dissipation layer by Vias connection.
PHASE_TPD	22	Phase Node pin. Used for heat transferring to heat dissipation layer by Vias connection.
GND_TPD	23, 25	Power ground pin. Connect to one or more ground plane directly and used for heat transferring to heat dissipation layer by Vias connection.
VOUT_TPD	24	Power output pin. Connect to output. Used for heat transferring to heat dissipation layer by Vias connection.

ELECTRICAL SPECIFICATIONS:

CAUTION: Do not operate at or near absolute maximum rating listed for extended periods of time. This stress may adversely impact product reliability and result in failures not covered by warranty.

Parameter	Description	Min.	Typ.	Max.	Unit
■ Absolute Maximum Ratings					
VIN to GND		-0.2	-	+40.0	V
SW to GND		-0.2		+40.0	V
EN to GND		-0.2	-	+40.0	V
Tc	Case Temperature of Inductor	-	-	+110	°C
Tj	Junction Temperature	-40	-	+150	°C
Tstg	Storage Temperature	-40	-	+125	°C
■ Recommendation Operating Ratings					
VIN	Input Supply Voltage	+4.5	-	+34.0	V
VOUT	Adjusted Output Voltage	+3.0		+12.0	V
Ta	Ambient Temperature	-40	-	+85	°C
■ Thermal Information					
Rth(j_{choke}-a)	Thermal resistance from junction to ambient (Note 1)	-	22	-	°C/W

NOTES:
1. Rth(j_{choke}-a) is measured with the component mounted on an effective thermal conductivity test board on 0 LFM condition. The test board size is 30mm×30mm×1.6mm with 4 layers, 2 oz per layer. The test condition is complied with JEDEC EIJ/JESD 51 Standards.

ELECTRICAL SPECIFICATIONS: (Cont.)

Conditions: T_A = 25 ºC, unless otherwise specified. Test Board Information: 30mm×30mm×1.6mm, 4 layers 2 oz. The output ripple and transient response measurement is short loop probing and 20MegHz bandwidth limited. Vin = 24V, Vout = 5.0V, Fsw=750k Hz, Cin =10uF/50V/1210/X7R, Cout = 22uF/16V/1210/X7R.

Symbol	Parameter	Conditions	Min.	Typ.	Max.	Unit
■ Input Characteristics						
I_{SD}	Input shutdown current	Vin =24V, EN = GND and no pull up resistance connect to VIN	-	1.2	-	uA
I_{IN}	Input supply bias current	Vin = 24V, Iout = 0A Vout = 5.0V, EN = VIN	-	200	-	uA
I_S	Input supply current	Vin = 24V, EN = VIN				
		Iout = 5mA,Vout =5.0V	-	1.9	-	mA
		Iout = 3A,Vout =5.0V	-	0.87	-	A
■ Output Characteristics						
$I_{OUT(DC)}$	Output continuous current range	Note 1.	0	-	3	A
$V_{O(SET)}$	Ouput Voltage Set Point	With 0.1% tolerance for external resistor used to set output voltage	-3	-	+3	% $V_{O(SET)}$
$\Delta V_{OUT}/\Delta V_{IN}$	Line regulation accuracy	Vin = 21.6V to 26.4V Vout = 5.0V, Iout = 3A	-	0.5	-	% $V_{O(SET)}$
$\Delta V_{OUT}/\Delta I_{OUT}$	Load regulation accuracy	Iout = 0A to 3A Vin = 24V, Vout = 5.0V	-	3	-	% $V_{O(SET)}$
$V_{OUT(AC)}$	Output ripple voltage	Vin = 24V, Vout = 5.0V EN = VIN, 20MHz Bandwidth	-	-	-	-
		IOUT = 5mA	-	15	-	mVp-p
		IOUT = 3A	-	45	-	mVp-p
■ Control Characteristics						
OCP	Protection Output Current	Note 2	3.3	-	5.5	A
OTP	Over temp protection			150		°C
F_{OSC}	Oscillator frequency (Frequency programmable)		0.5	-	1.1	MHz
V_{ENL}	EN Low threshold		0.4	-	-	V
V_{ENH}	EN High Threshold		-	-	1.7	V
UVLO	Input under voltage lockout threshold				4.5	V

NOTES :

2. V_{IN}=24V, V_{OUT}=12V, I_{OUT}=2.4A MAX

TYPICAL PERFORMANCE CHARACTERISTICS: 5.0Vout

Conditions: T_A = 25 ºC, unless otherwise specified. Test Board Information: 30mm×30mm×1.6mm, 4 layers 2 oz.
The output ripple and transient response measurement is short loop probing and 20MegHz bandwidth limited.
Fsw=750k Hz, Cin =10uF/50V/1210/X7R, Cout = 22uF/16V/1210/X7R.
The following figures provide the typical characteristic curves at 5.0Vout.

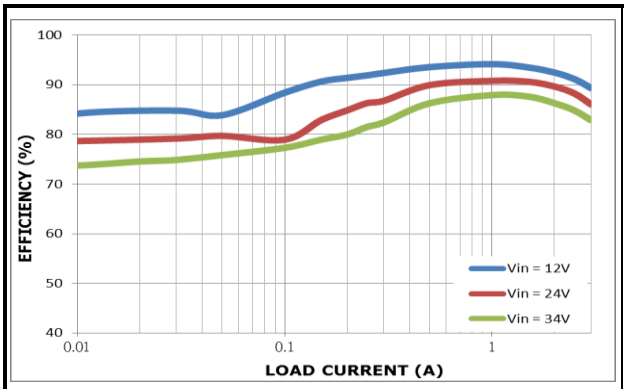


FIG.3 5VOUT EFFICIENCY V.S. LOAD CURRENT

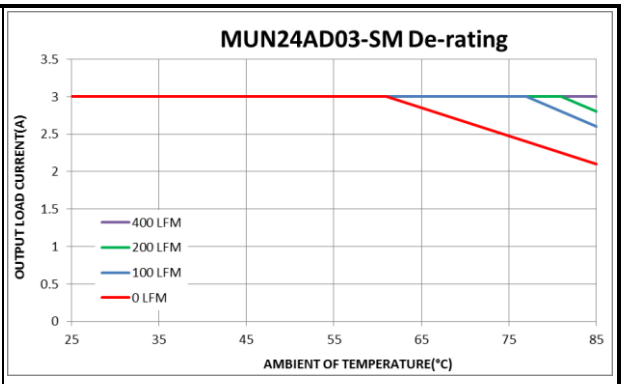


FIG.4 DE-RATING CURVE AT 24VIN

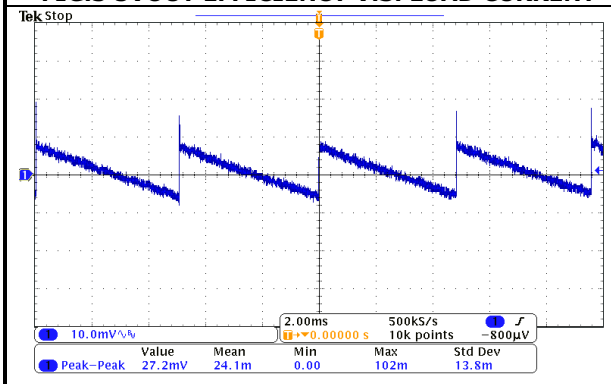


FIG.5 OUTPUT RIPPLE
(24VIN, 5VOUT, IOUT=0A)

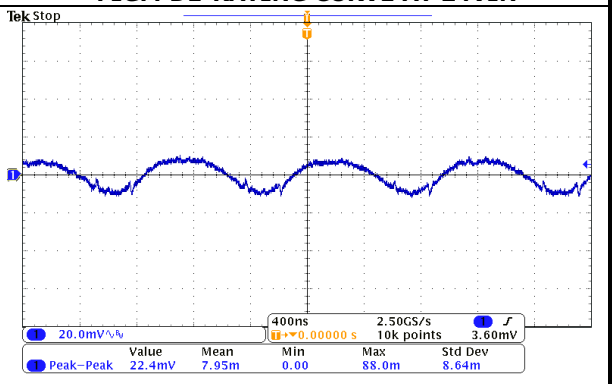


FIG.6 OUTPUT RIPPLE
(24VIN, 5VOUT, IOUT=3A)

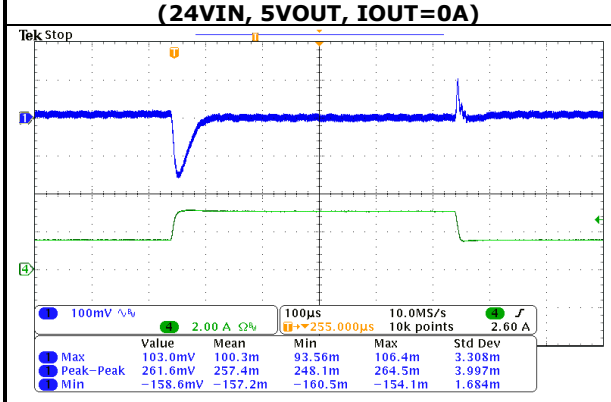


FIG.7 TRANSIENT RESPONSE
(24VIN, 5VOUT, 1.5A to 3A LOAD STEP)

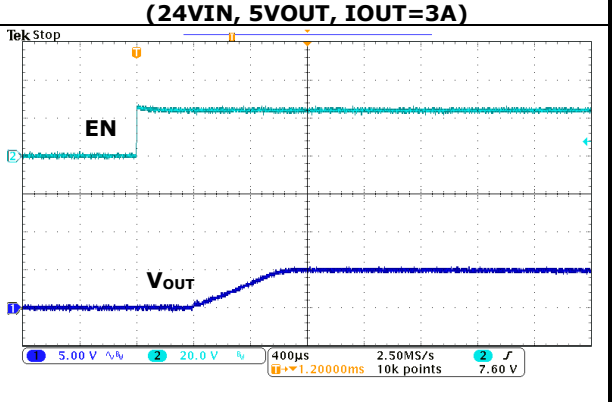


FIG.8 TURN-ON
(24VIN, 5VOUT, IOUT=3A)

TYPICAL PERFORMANCE CHARACTERISTICS: 12.0Vout

Conditions: T_A = 25 ºC, unless otherwise specified. Test Board Information: 30mm×30mm×1.6mm, 4 layers 2 oz.
The output ripple and transient response measurement is short loop probing and 20MegHz bandwidth limited.
Fsw=750k Hz, Cin =10uF/50V/1210/X7R, Cout = 22uF/16V/1210/X7R.
The following figures provide the typical characteristic curves at 12.0Vout.

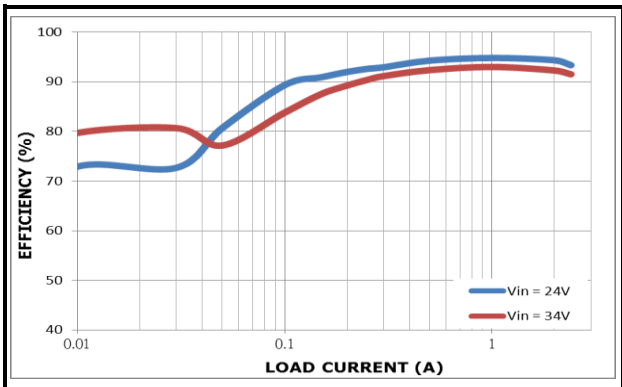


FIG.9 12VOUT EFFICIENCY V.S. LOAD CURRENT

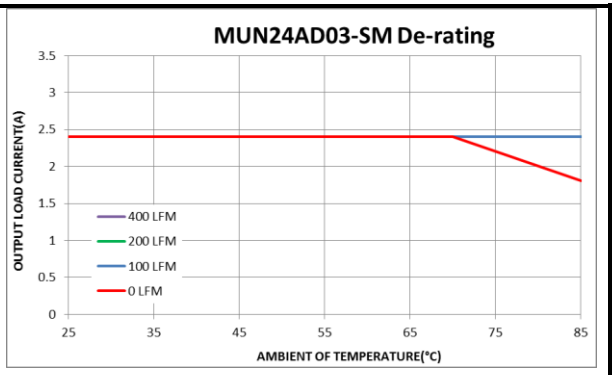


FIG.10 DE-RATING CURVE AT 24VIN

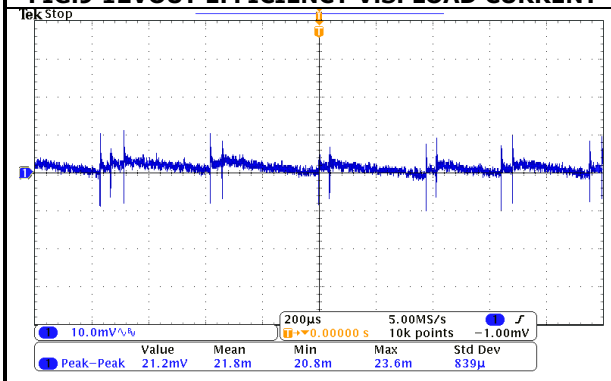


FIG.11 OUTPUT RIPPLE
(24VIN, 12VOUT, IOUT=0A)

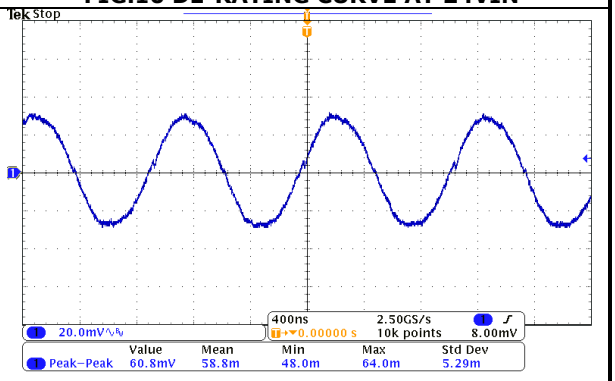


FIG.12 OUTPUT RIPPLE
(24VIN, 12VOUT, IOUT=2.4A)

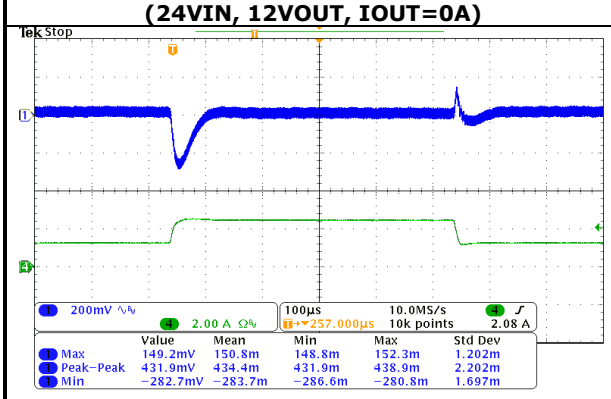


FIG.13 TRANSIENT RESPONSE
(24VIN, 12VOUT, 1.2A to 2.4A LOAD STEP)

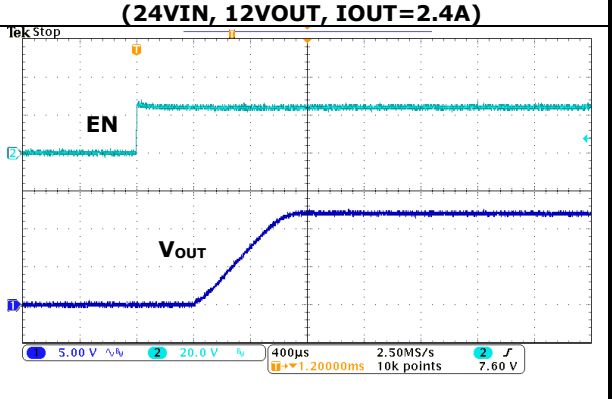


FIG.14 TURN-ON
(24VIN, 12VOUT, IOUT=2.4A)

APPLICATIONS INFORMATION: (Cont.)

SAFETY CONSIDERATIONS:

Certain applications and/or safety agencies may require fuses at the inputs of power conversion components. Fuses should also be used when there is the possibility of sustained input voltage reversal which is not current limited. For greatest safety, we recommend a fast blow fuse installed in the ungrounded input supply line. The installer must observe all relevant safety standards and regulations. For safety agency approvals, install the converter in compliance with the end-user safety standard.

INPUT FILTERING:

The module should be connected to as low AC impedance source supply and a highly inductive source or line inductance can affect the stability of the module. Input capacitors must be placed directly to the input pin of the module, to minimize input ripple voltage and ensure module stability.

OUTPUT FILTERING:

To reduce output ripple and improve the dynamic response to as step load change, the additional capacitors at the output must be used. Low ESR ceramic capacitors are recommended to improve the output ripple and dynamic response of the module.

PROGRAMMING OUTPUT VOLTAGE:

The module has an internal 0.6V±1.5% reference voltage. The output voltage can be programmed by the dividing resistor R_{FB} which respects to FB pin and GND pin. The output voltage should be considered by convert ratio by $Toff_{MIN}$ and Ton_{MIN} and the resistance according to typical output voltage is shown in TABLE 1.

$$VOUT\ (V) = 0.6 \times \left(1 + \frac{100k}{R_{FB}}\right) \qquad \text{(EQ.1)}$$

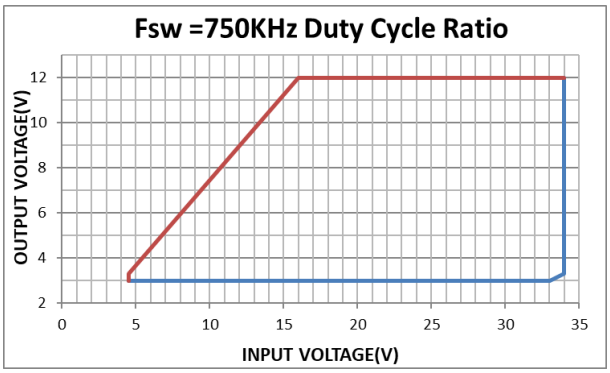
TABLE 1: OUTPUT VOLTAGE SETTING

Vout	3.3	5V	9V	12V
RFB (Ohm)	22.22k	13.636k	7.142k	5.263k

Note. R_{FB1} maximum 200 Kohm, minimum 10 Kohm.

APPLICATIONS INFORMATION: (Cont.)

DUTY CYCLE RATIO OF APPLICATION :



THERMAL CONSIDERATIONS:

All of thermal testing condition is complied with JEDEC EIJ/JESD 51 Standards. Therefore, the test board size is 30mm×30mm×1.6mm with 4 layers. The case temperature of module sensing point is shown as FIG.15 Then Rth(j_{choke}-a) is measured with the component mounted on an effective thermal conductivity test board on 0 LFM condition. The MUN24AD03-SM module is designed for using when the case temperature is below 110°C regardless the change of output current, input/output voltage or ambient temperature.

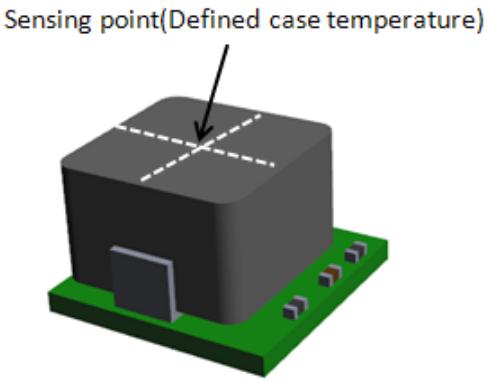


FIG.15 Case Temperature Sensing Point

APPLICATIONS INFORMATION: (Cont.)

LAYOUT RECOMMENDATIONS:

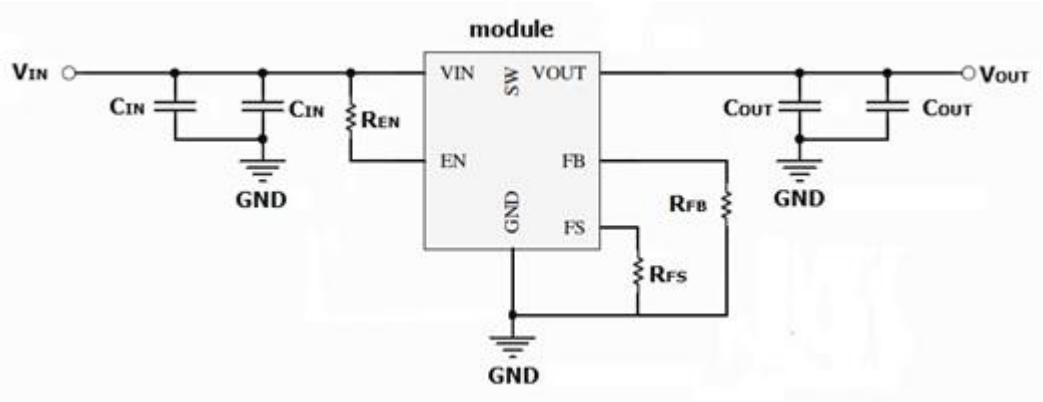


FIG.16 Circuit Of Layout

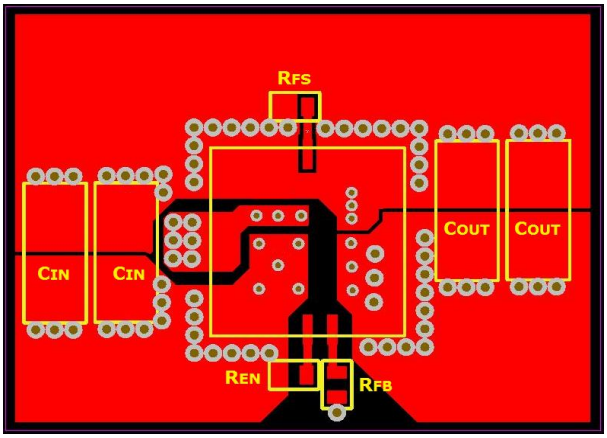


FIG.17 Layout Of First Layer

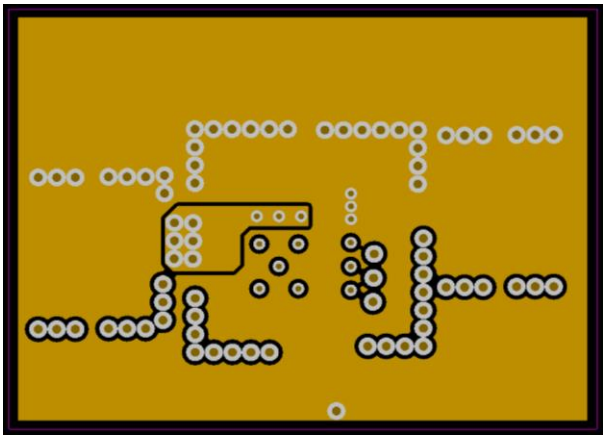


FIG.18 Layout Of Second Layer

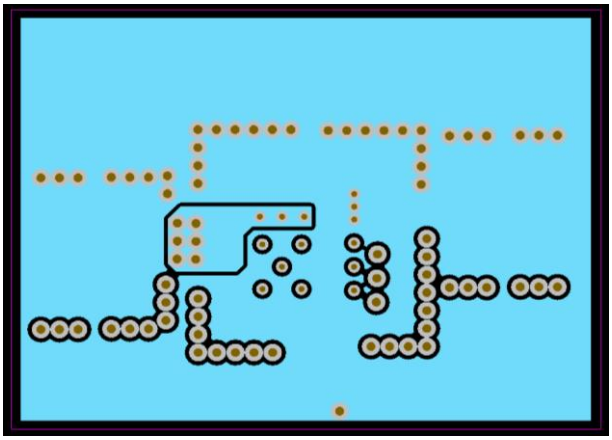


FIG.19 Layout Of Third Layer

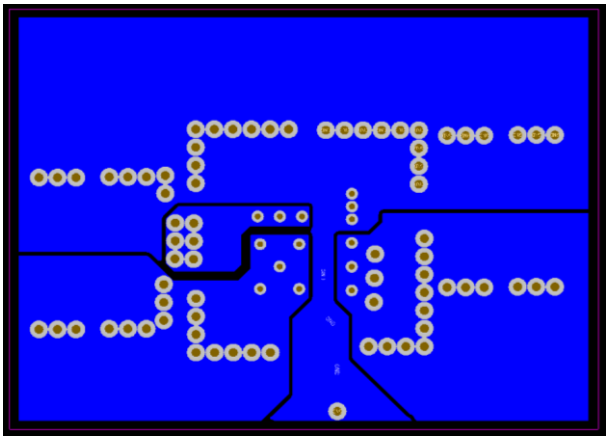


FIG.20 Layout Of Fourth Layer

APPLICATIONS INFORMATION: (Cont.)

REFLOW PARAMETERS:

Lead-free soldering process is a standard of electronic products production. Solder alloys like Sn/Ag, Sn/Ag/Cu and Sn/Ag/Bi are used extensively to replace the traditional Sn/Pb alloy. Sn/Ag/Cu alloy (SAC) is recommended for this power module process. In the SAC alloy series, SAC305 is a very popular solder alloy containing 3% Ag and 0.5% Cu and easy to obtain. Figure 21 shows an example of the reflow profile diagram. Typically, the profile has three stages. During the initial stage from room temperature to 150°C, the ramp rate of temperature should not be more than 3°C/sec. The soak zone then occurs from 150°C to 200°C and should last for 60 to 120 seconds. Finally, keep at over 217°C for 60 ~150 seconds to melt the solder and make the peak temperature at the range from 245°C to 250°C. It is noted that the time of peak temperature should depend on the mass of the PCB board. The reflow profile is usually supported by the solder vendor and one should adopt it for optimization according to various solder type and various manufacturers' formulae.

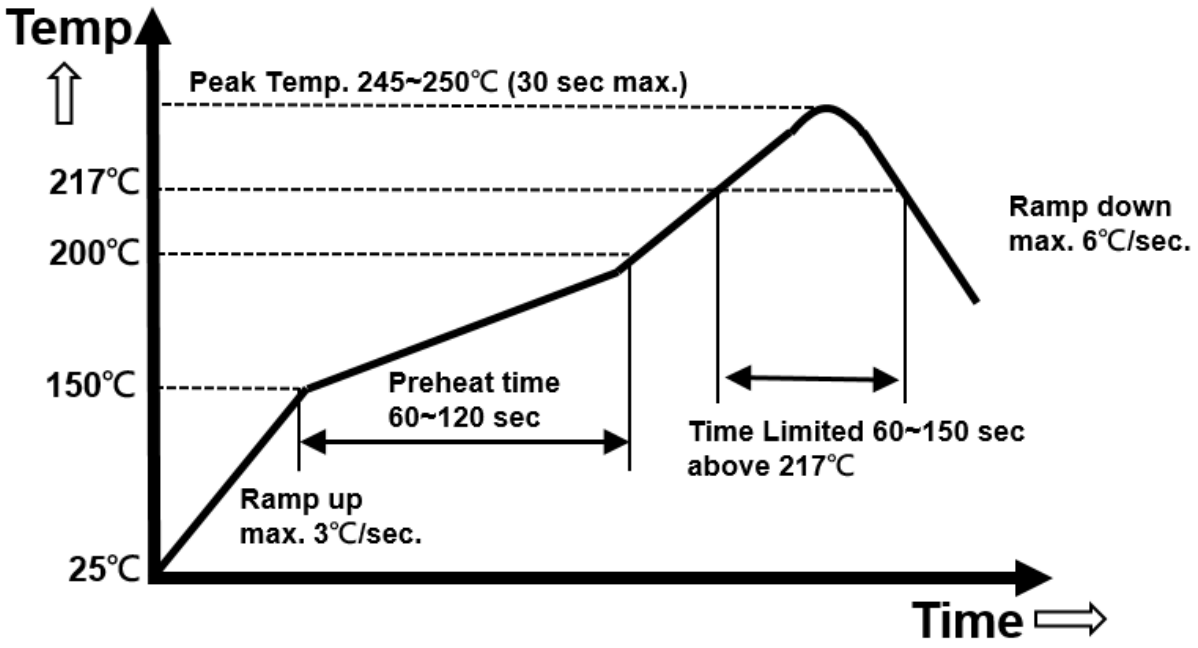
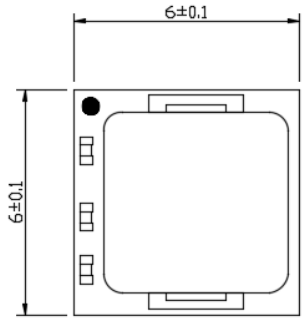


FIG.21 RECOMMENDATION REFLOW PROFILE

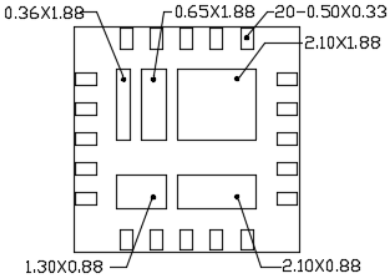
PACKAGE OUTLINE DRAWING:

unit: mm

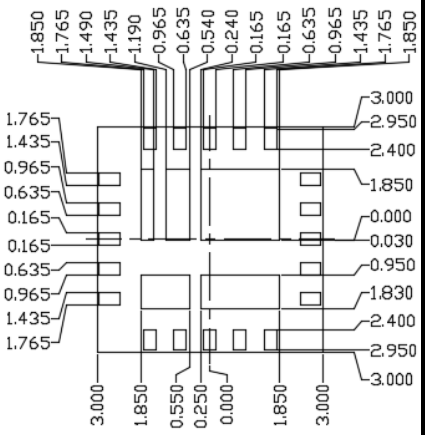
General Tolerance: ±0.1mm



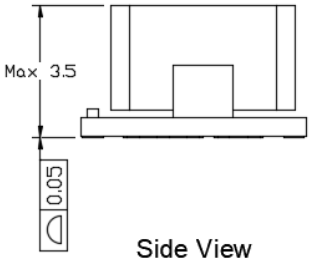
Top View



Bottom View



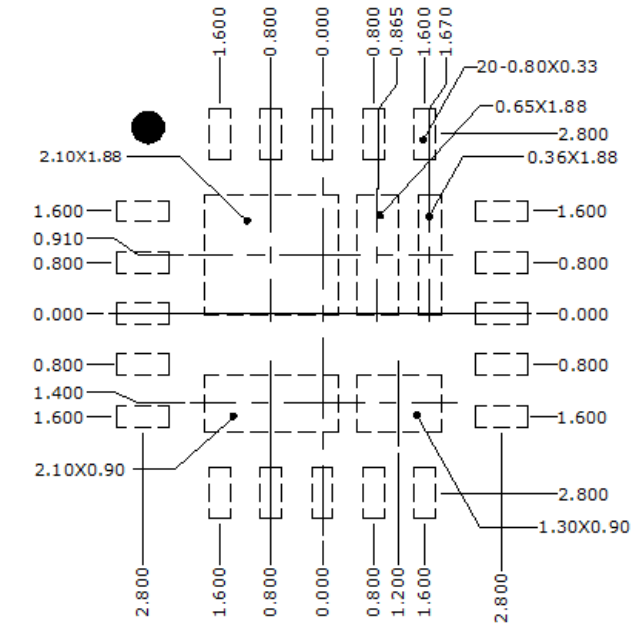
Bottom View



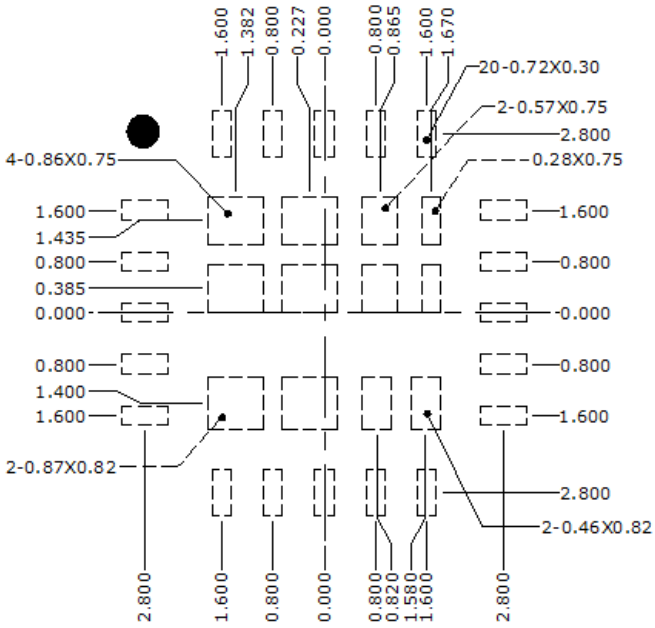
Side View

LAND PATTERN REFERENCE:

Unit:mm



RECOMMENDED LAND PATTERN



RECOMMENDED STENCIL PATTERN*

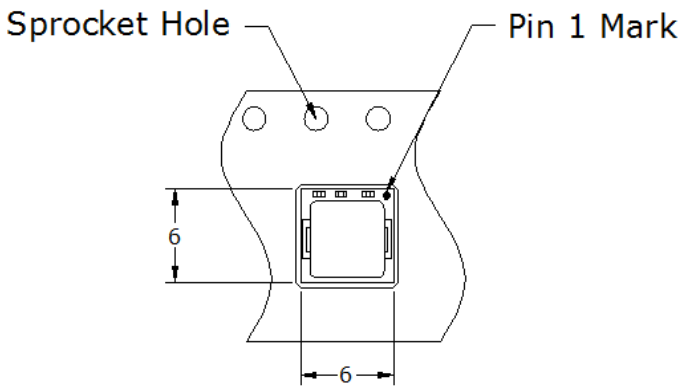
*Based on 0.1~0.15mm thickness stencil (Reference only)

*Recommended solder paste coverage 55~100%

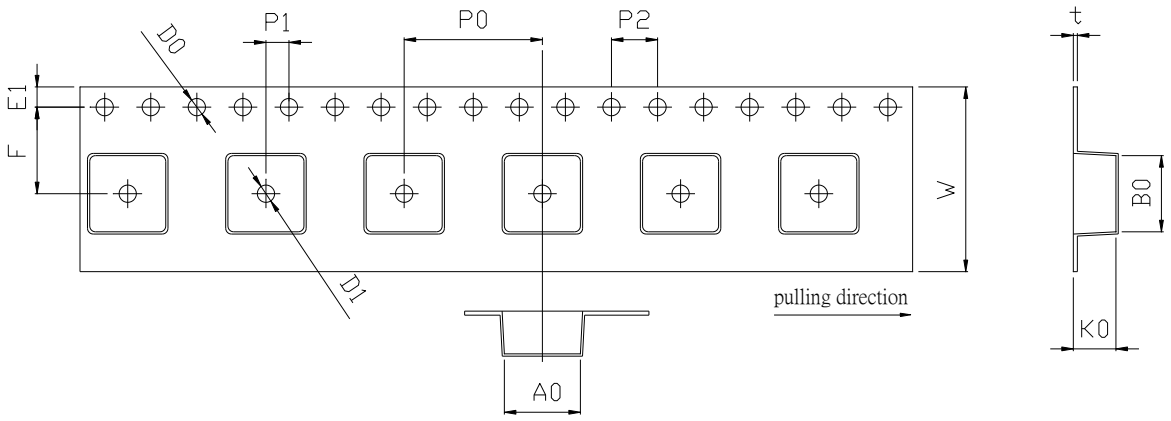
PACKING REFERENCE:

Unit: mm

Package In Tape Loading Orientation



Tape Dimension

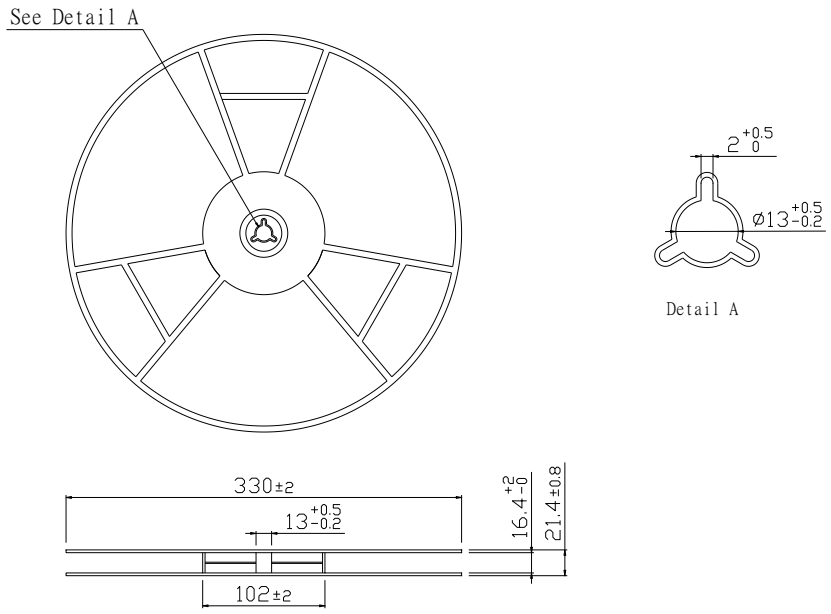


A0	6.60 ± 0.10	E1	1.75 ± 0.10
B0	6.60 ± 0.10	K0	3.70 ± 0.10
F	7.50 ± 0.10	P0	12.00 ± 0.10
W	16.00 ± 0.30	P1	2.00 ± 0.10
D0	φ1.5 +0.1/-0.0	P2	4.00 ± 0 10
D1	φ1.5 Min.	t	0.35 ± 0.05

PACKING REFERENCE: (Cont.)

Unit: mm

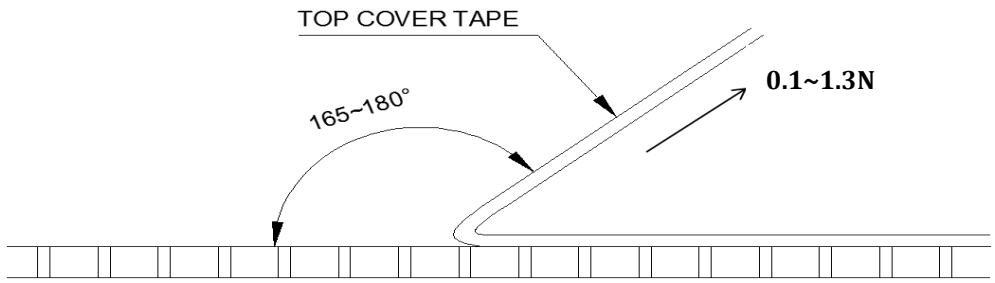
Reel Dimension



Peel Strength of Top Cover Tape

The peel speed shall be about 300mm/min.

The peel force of top cover tape shall be between 0.1N to 1.3N



REVISION HISTORY:

Date	Revision	Changes
2015.09.11	00	Issue initial preliminary datasheet
2015.10.27	01	1. Change MSL level from level 2 to level 3 2. Update Page 4~5 electrical specifications 3. Change page 6~8 de-rating curve for 4 layer 1oz EVB 4. Update page 9 output voltage setting table 5. Add page 10~11 layout recommendations 6. Add page 12 reflow parameters
2015.11.26	02	Update page 12 reflow parameters
2015.12.07	03	Update page 3 pin description of FS
2016.09.29	04	1. Change MSL level from level 3 to level 2 on page 1 and 2 2. Change page 4~7 test condition and electrical spec.(EVB 1oz change to 2oz, OCP typ. Value change to Min. and Max. value. 3. Update page 13 land pattern reference
2018.02.21	05	1. Change page 5 EN Low threshold from max 0.8V to min 0.4V
2021.02.15	06	1. Change Output voltage range to 3V from 5V 2. Update FS pin description
2022.03.29	07	1. Update application circuit for EN pin adding a 0.1uF ceramic capacitor to GND 2. Update mechanical and POD drawing. 3. Update reflow parameters information.
2022.06.01	A0	1. Update land pattern information