Cyntec Power Module Solutions for FPGA

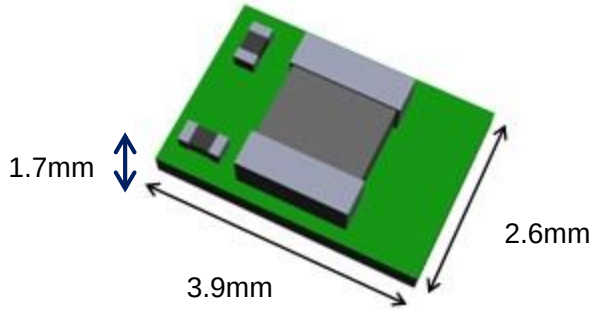
MUN12AD01-SG

Cyntec Co., Ltd.

MUN12AD01-SG FEATURE & APPLICATION

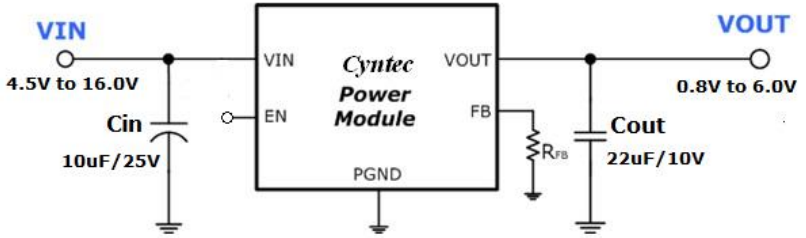
FEATURES:

- High Density Fully Integration Module
- 1000mA Output Current
- Input Voltage Range from 4.5V to 16.0V
- Output Voltage Range from 0.8V to 6.0V
- 94% Peak Efficiency at 5 Vin to 3.3 Vout
- Force PWM mode
- Enable Function
- Protections (UVLO, OCP: Non-latching)
- Internal Soft Start
- Compact Size: 3.9mm*2.6mm*1.7mm
- Pb-free for RoHS compliant
- MSL 2, 260°C Reflow



APPLICATIONS:

- DSL Modem / LCD TV
- Portable TV / Access Point Router



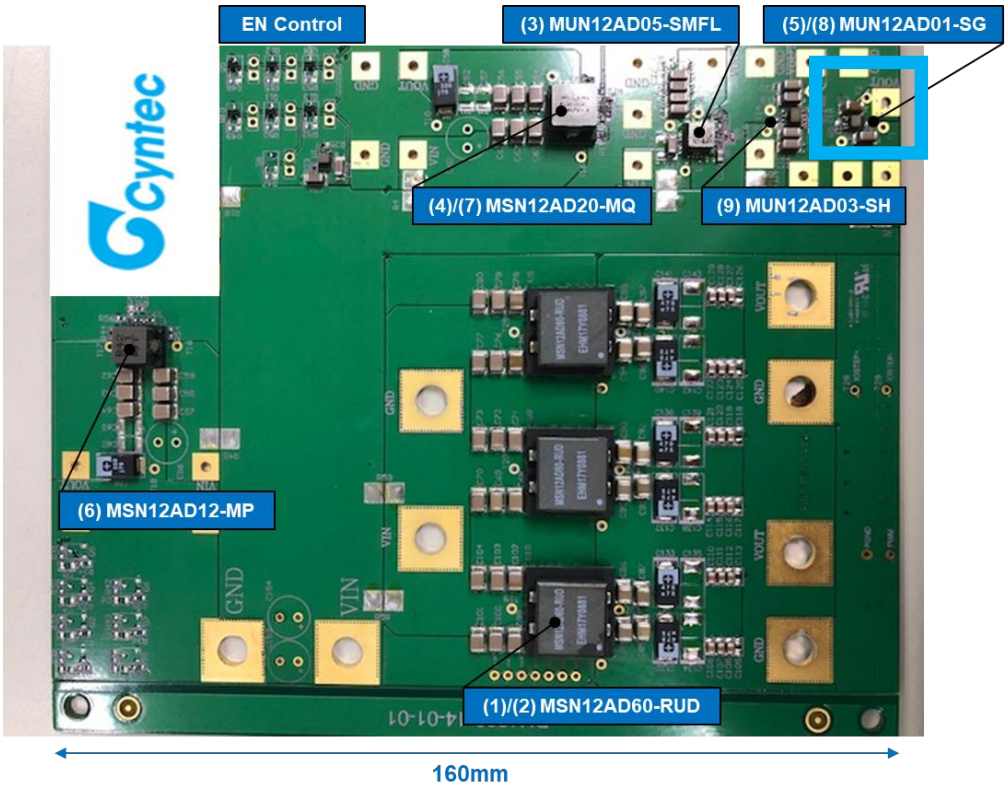
Specifications

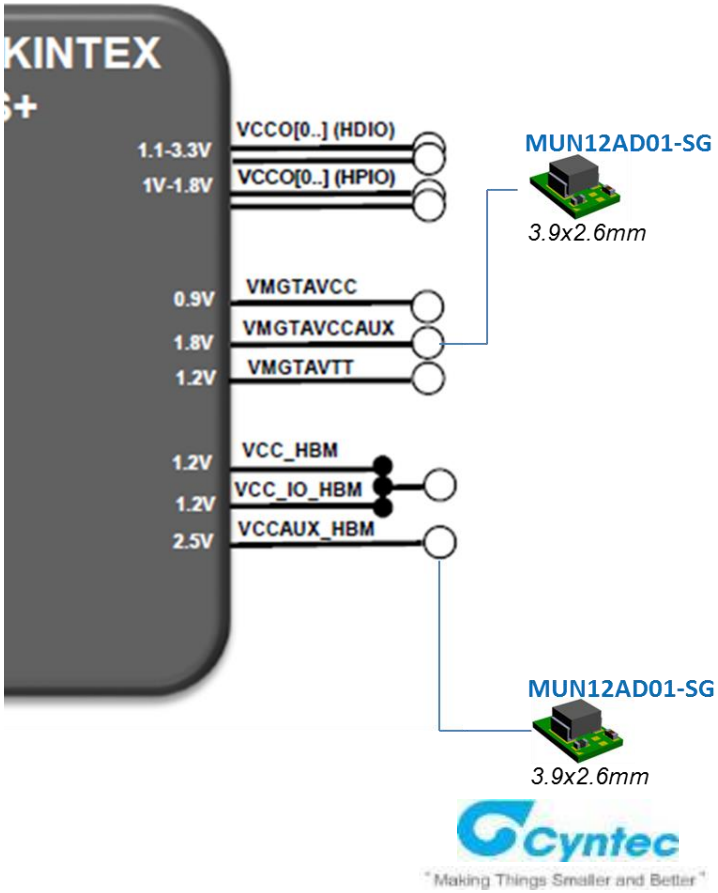
VMGTAVCCAUX

- 1.8V, current 0.1~0.5A
- <10mV$_{pk-pk}$ from 10kHz to 80MHz (UG578)

VCCAUX_HBM

- 2.5V, current 0.4A





MUN12AD01-SG for Xilinx XCVU13P
Efficiency (1.8Vout)

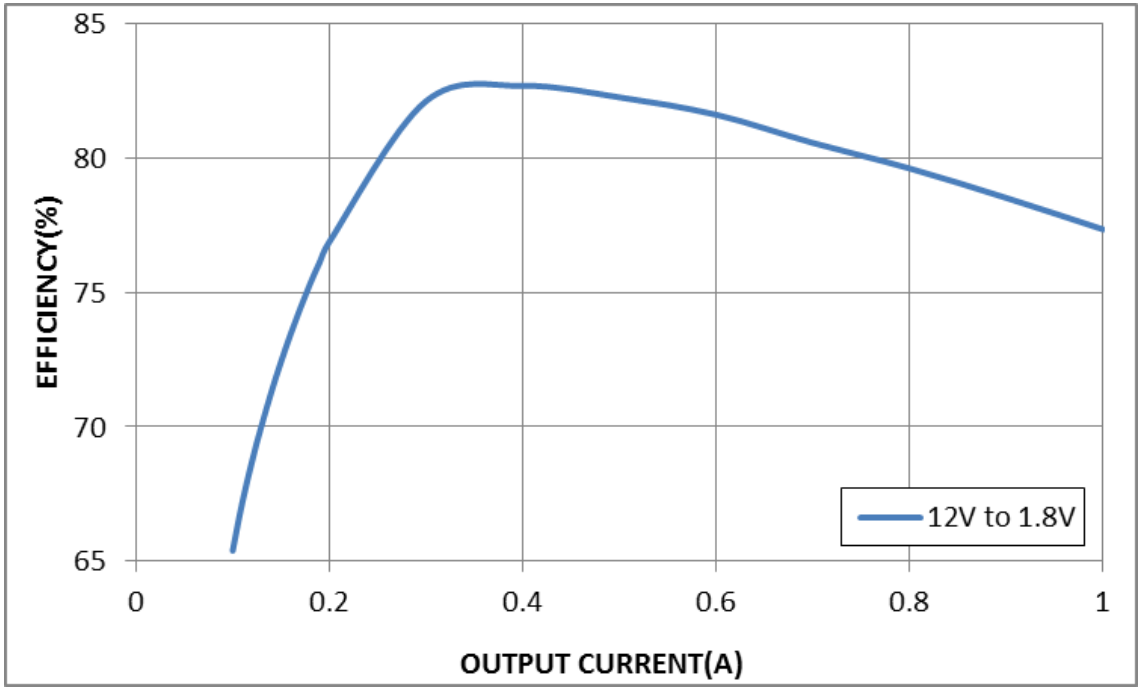
Test Condition

VIN=12V VOUT=1.8V IOUT=1A

Module: Cyntec MUN12AD01-SG

Input Capacitor: 10uF

Output Capacitor: 22uF



VOUT=1.8V Pk-Pk Efficiency= 82.6% for IOUT=0.4A

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MUN12AD01-SG for Xilinx XCVU13P
Ripple (1.8Vout)

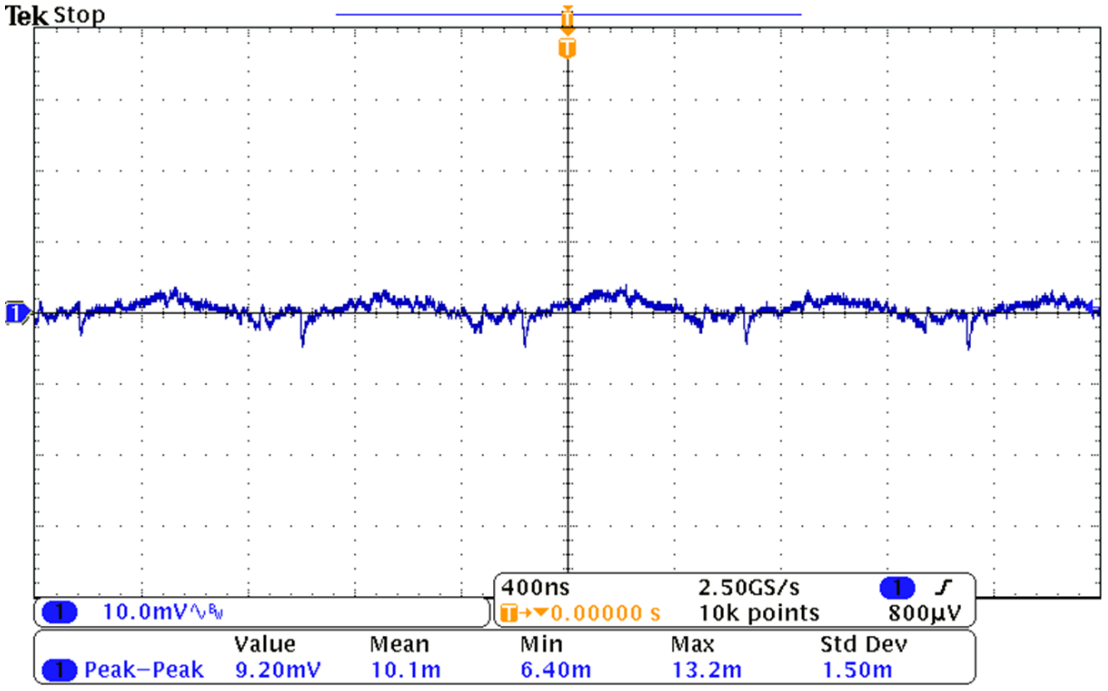
Test Condition

VIN=12V VOUT=1.8V IOUT=1A

Module: Cyntec MUN12AD01-SG

Input Capacitor: 10uF

Output Capacitor: 22uF



VOUT=1.8V Pk-Pk 9.2mV for IOUT=1A

MUN12AD01-SG for Xilinx XCVU13P
Transient (1.8Vout)

Test Condition

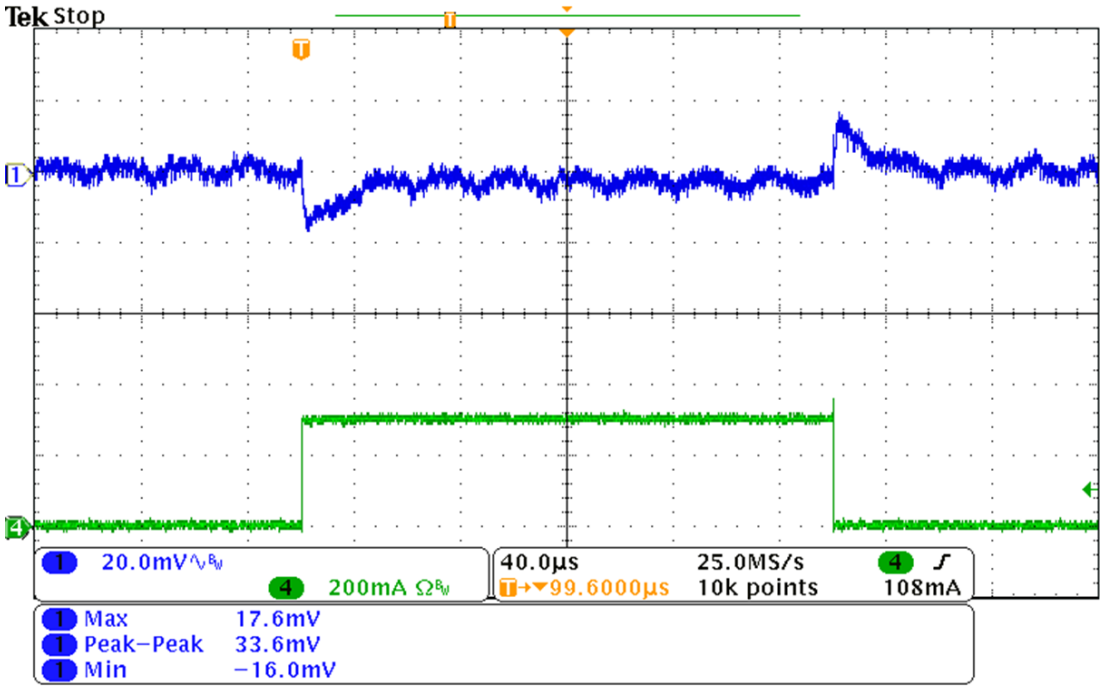
VIN=12V VOUT=1.8V IOUT=1A

Module: Cyntec MUN12AD01-SG

Input Capacitor: 10uF

Output Capacitor: 22uF

Transient < ± 3%, Io=0A~0.3A, 10A/us with output



VOUT=1.8V Pk-Pk Transient =33.6mV for IOUT=0~0.3A

MUN12AD01-SG for Xilinx XCVU13P
Thermal (1.8Vout)

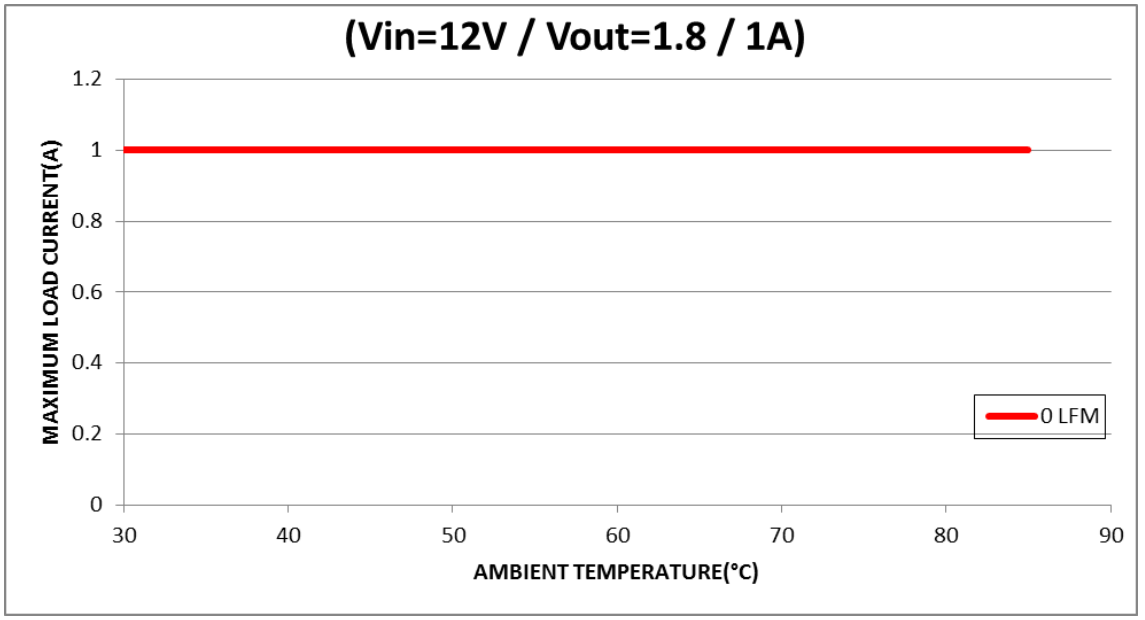
Test Condition

VIN=12V VOUT=1.8V IOUT=1A

Module: Cyntec MUN12AD01-SG

Input Capacitor: 10uF

Output Capacitor: 22uF



0 LFM No De-rating

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MUN12AD01-SG for Xilinx XCVU13P
Efficiency (2.5Vout)

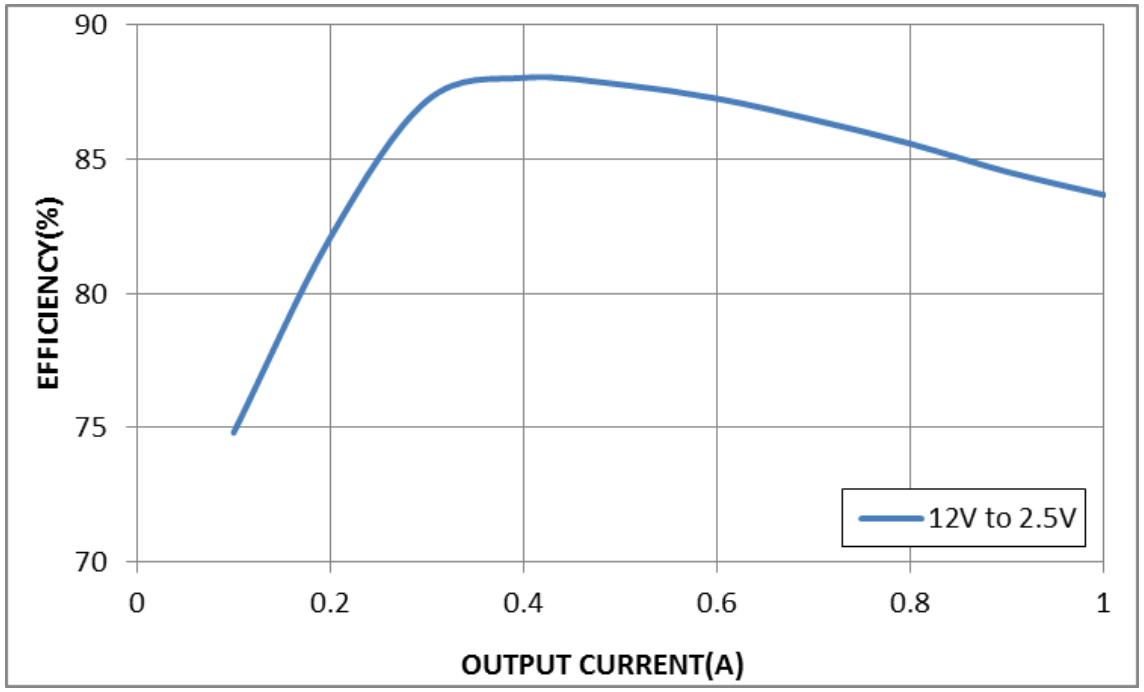
Test Condition

VIN=12V VOUT=2.5V IOUT=1A

Module: Cyntec MUN12AD01-SG

Input Capacitor: 10uF

Output Capacitor: 47uF



VOUT=2.5V Pk-Pk Efficiency= 88% for IOUT=0.4A

MUN12AD01-SG for Xilinx XCVU13P
Ripple (2.5Vout)

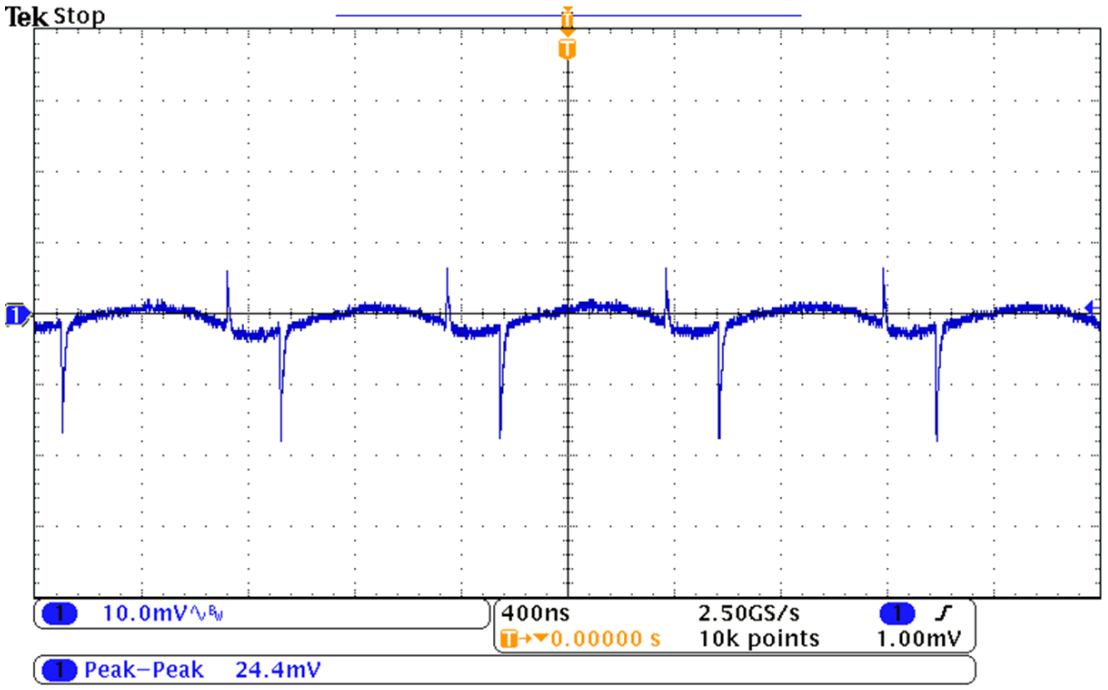
Test Condition

VIN=12V VOUT=2.5V IOUT=1A

Module: Cyntec MUN12AD01-SG

Input Capacitor: 10uF

Output Capacitor: 47uF



VOUT=2.5V Pk-Pk 24.4mV for IOUT=1A

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MUN12AD01-SG for Xilinx XCVU13P
Transient (2.5Vout)

Test Condition

VIN=12V VOUT=2.5V IOUT=1A

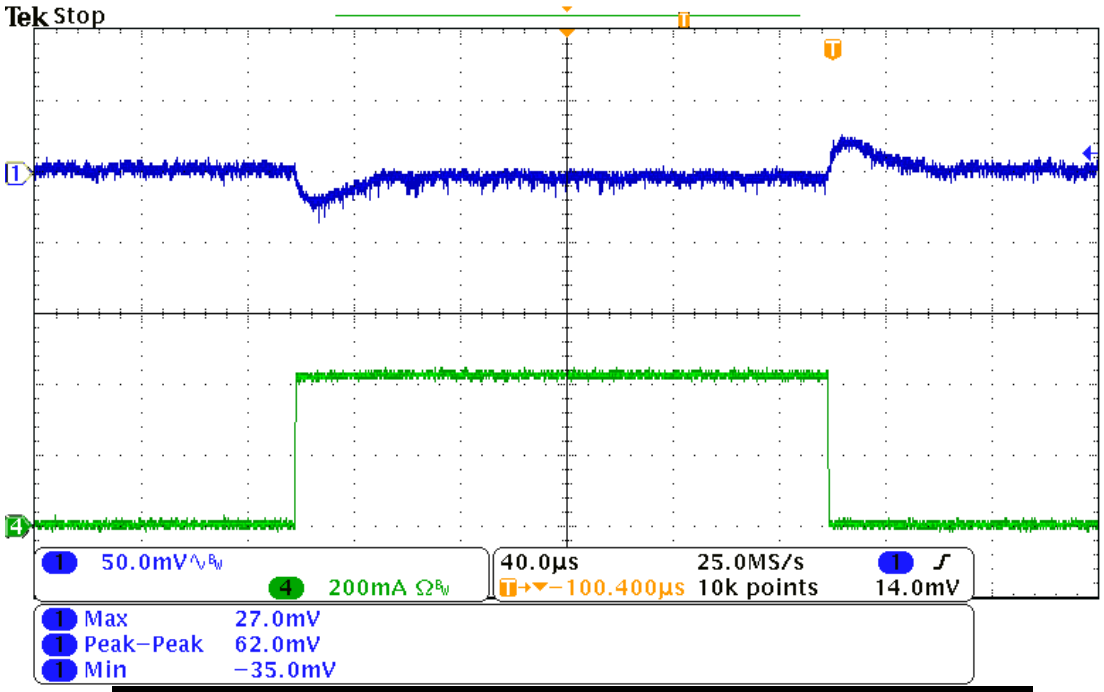
Module: Cyntec MUN12AD01-SG

CFB = 100pF

Input Capacitor: 10uF

Output Capacitor: 47uF

Transient < ± 3%, Io=0A~0.4A, 10A/us



VOUT=2.5V Pk-Pk Transient =62mV for IOUT=0~0.4A

MUN12AD01-SG for Xilinx XCVU13P
Thermal (2.5Vout)

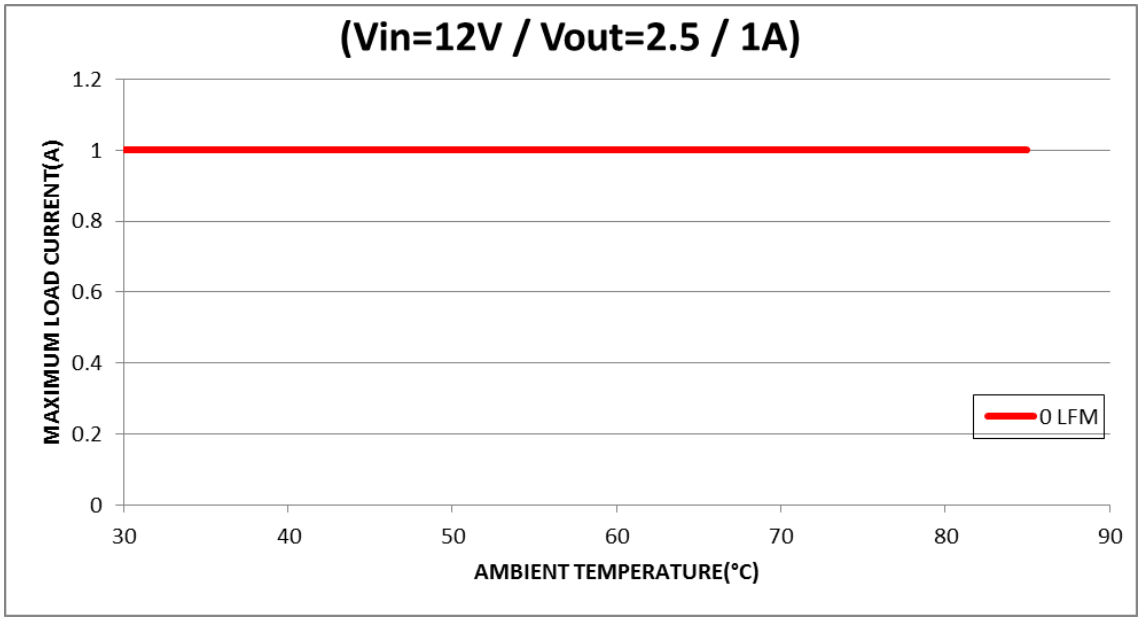
Test Condition

VIN=12V VOUT=2.5V IOUT=1A

Module: Cyntec MUN12AD01-SG

Input Capacitor: 10uF

Output Capacitor: 47uF

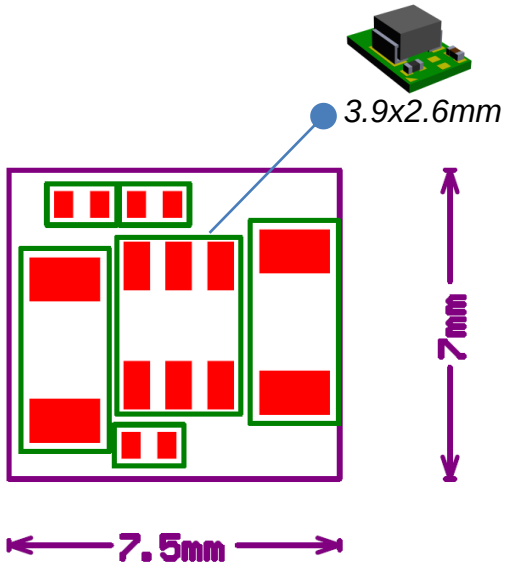


0 LFM No De-rating

Layout Example of the 1A module

(Layout is for reference only --- single-sided SMT. Further optimization is possible in terms of output characteristics and actual application environment)

MUN12AD01-SG



Remarks

- Input capacitance: 10uF
- Output capacitance: 47uF
- Arrangement could be optimized based on output transient requirements