

Cyntec Power Module Solutions for FPGA

MUN12AD03-SH

Cyntec Co., Ltd.



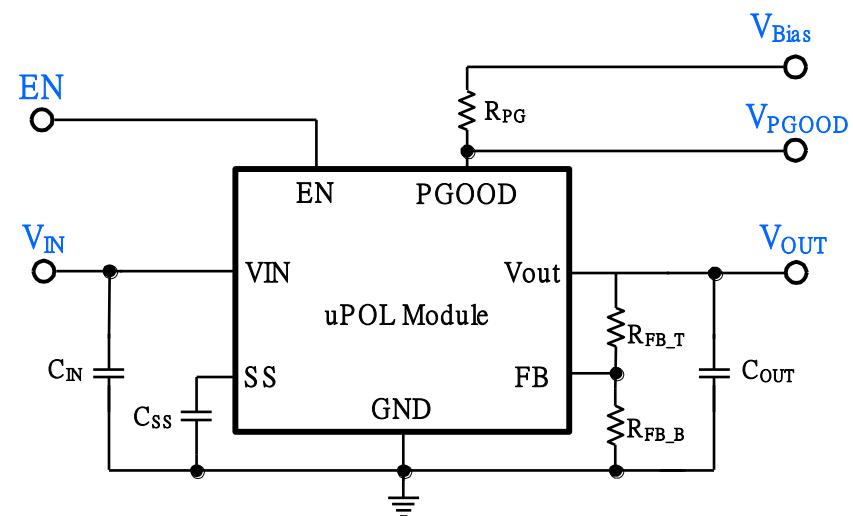
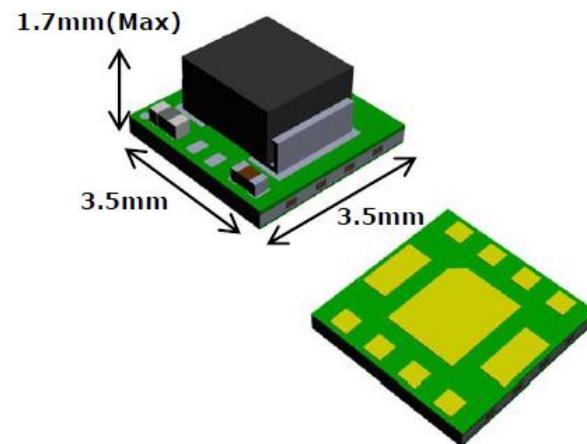
MUN12AD03-SH FEATURE & APPLICATION

FEATURES:

- High Density uPOL Module
- 3A Output Current
- 91% Peak Efficiency at 12VIN
- Input Voltage Range from 4.5V to 16V
- Output Voltage Range from 0.6V to 5.0V
- Enable / PGOOD Function
- Automatic Power Saving/PWM Mode
- Protections (OCP: Non-latching, OTP)
- Adjustable Soft Start Function
- Compact Size: 3.5mm*3.5mm*1.7mm
- Pb-free for RoHS compliant
- MSL 2, 260°C Reflow

APPLICATIONS:

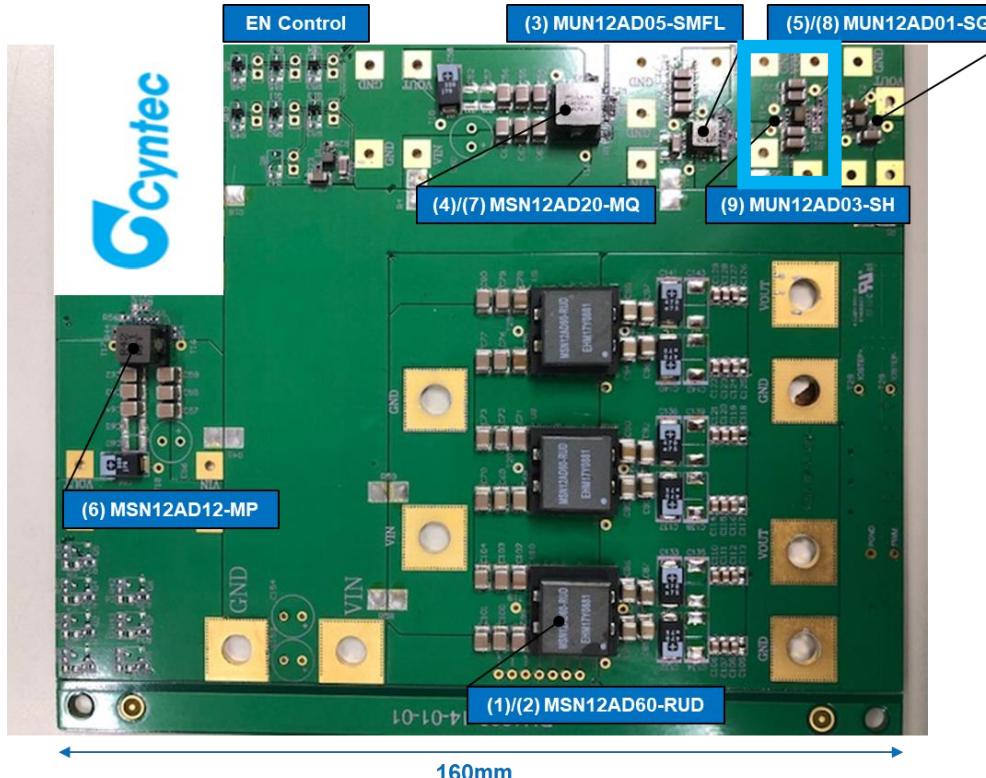
- Point of Load Conversion
- LDOs Replacement
- Set Top Box / DSL Modem / AP Router
- Industrial Personal Computer



Specifications

VCC_IO

- 1.8V/2.5V/3.3V, current ~3A



MUN12AD03-SH for Xilinx XCVU13P

Efficiency

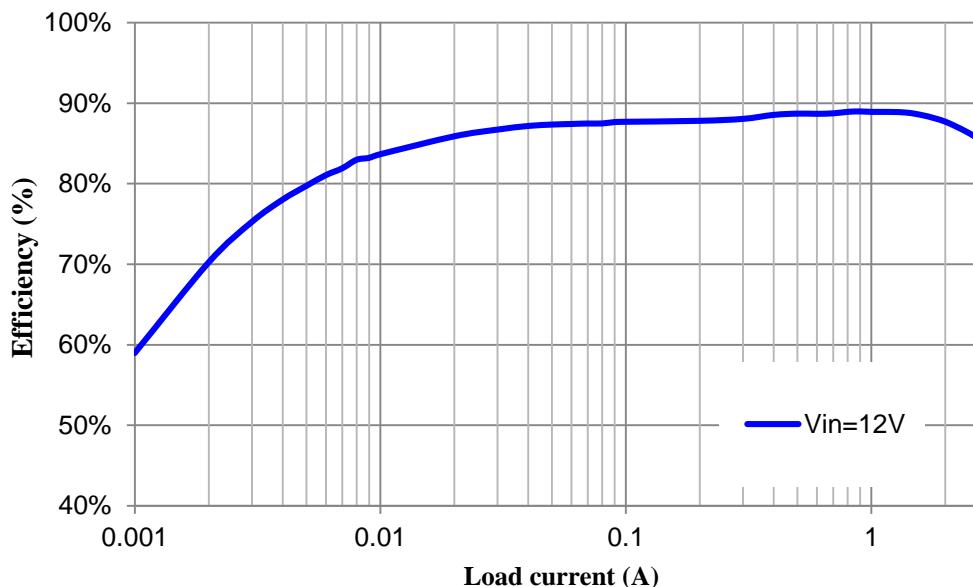
Test Condition

VIN=12V VOUT=3.3V IOUT=3A

Module: Cyntec MUN12AD03-SH

Input Capacitor: 22uF x 1pcs

Output Capacitor: 47uF x 2pcs



VOUT=3.3V Pk Efficiency= 89% at IOUT=1A

MUN12AD03-SH for Xilinx XCVU13P

Ripple

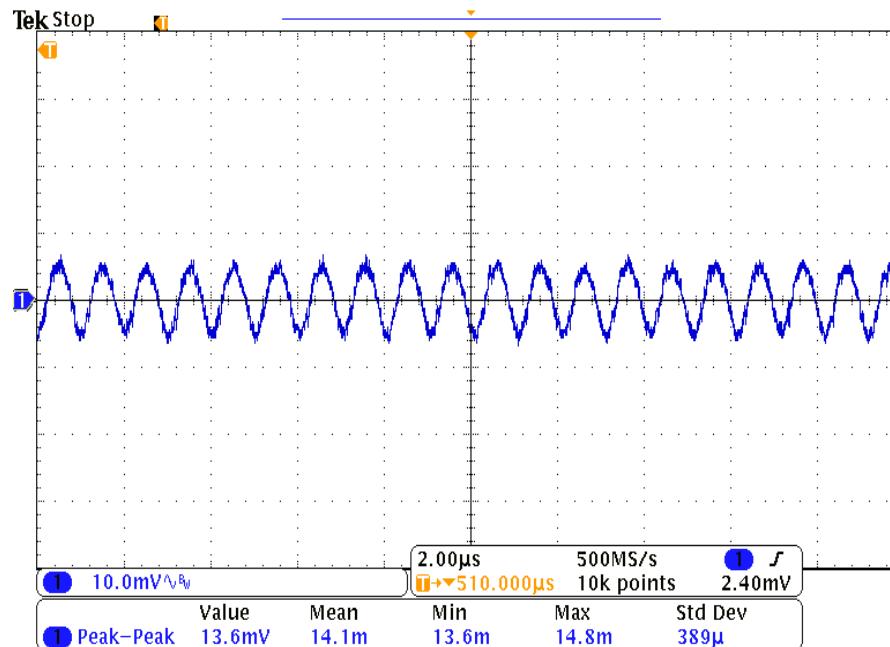
Test Condition

VIN=12V VOUT=3.3V IOUT=3A

Module: Cyntec MUN12AD03-SH

Input Capacitor: 22uF x 1pcs

Output Capacitor: 47uF x 2pcs



VOUT=0.85V Pk-Pk 13.6mV for IOUT=3A

MUN12AD03-SH for Xilinx XCVU13P Transient

Test Condition

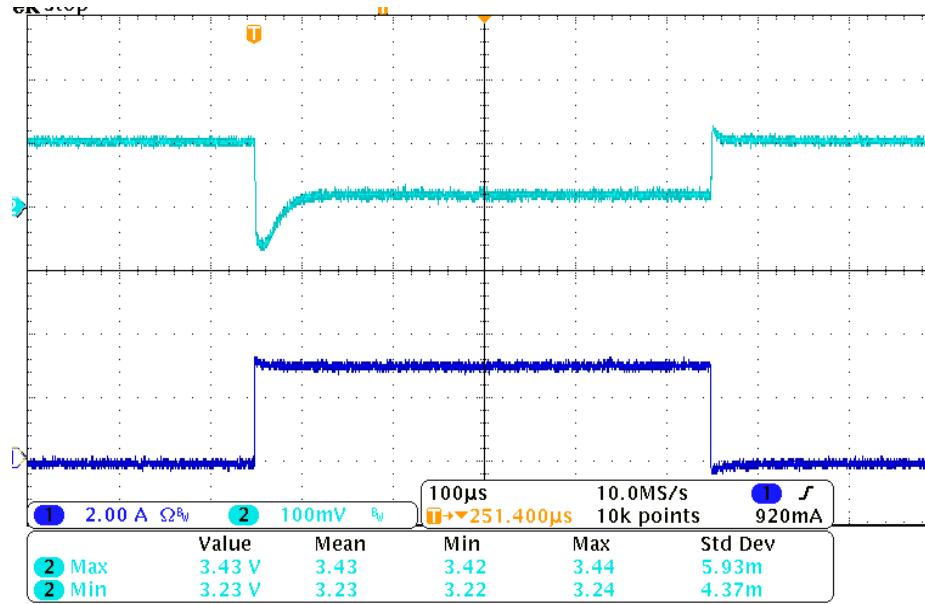
VIN=12V VOUT=3.3V IOUT=3A

Module: Cyntec MUN12AD03-SH

Input Capacitor: 22uF x 1pcs

Output Capacitor: 47uF x 2pcs

Transient < ± 5% at 90% step (0-2.7A), 10A/us with output capacitance 2x47uF



VOUT=3.3V Pk-Pk Transient =200mV for IOUT=0~2.7A

MUN12AD03-SH for Xilinx XCVU13P

Thermal

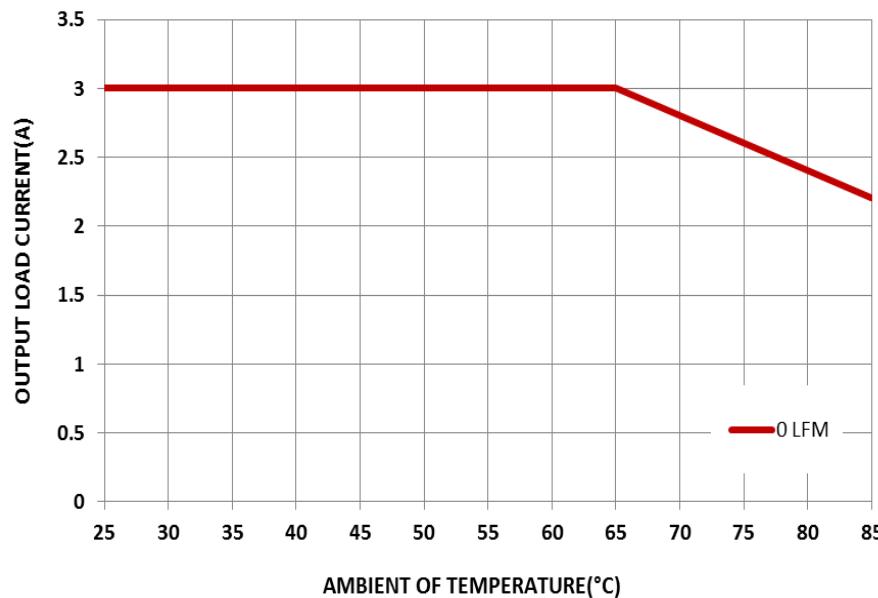
Test Condition

VIN=12V VOUT=3.3V IOUT=3A

Module: Cyntec MUN12AD03-SH

Input Capacitor: 22uF x 1pcs

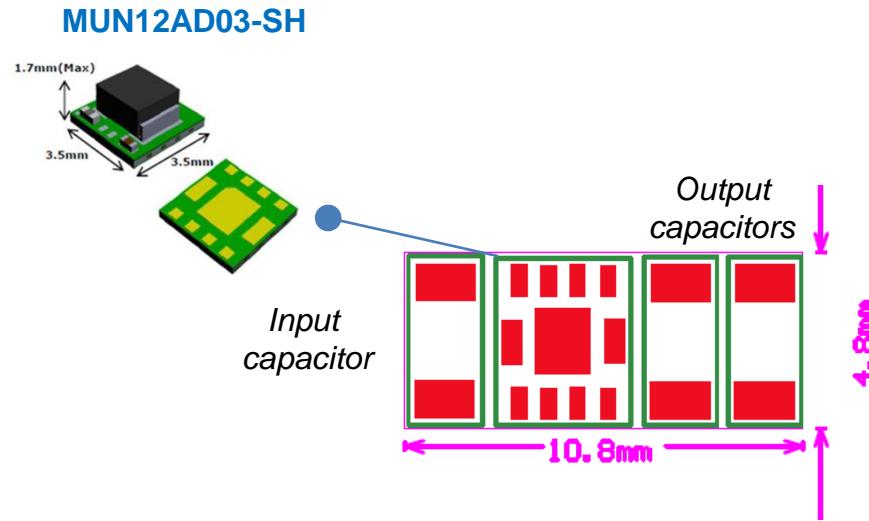
Output Capacitor: 47uF x 2pcs



65°C De-rating

Layout Example of the 3A module

(Layout is for reference only --- single-sided SMT. Further optimization is possible in terms of output characteristics and actual application environment)



Remarks

- Input capacitance: 22uF
- Output capacitance: 47uF x2pcs
- Arrangement could be optimized based on output transient requirements