uPOL Module

3A, High Efficiency uPOL Module

MUN12AD03-SM

FEATURES:

- High Density uPOL Module
- 3A Output Current
- Input Voltage Range from 4.5V to 16V
- Output Voltage Range from 0.6V to 5.0V
- 93% Peak Efficiency at 12VIN
- Enable / PGOOD Function
- Automatic Power Saving/PWM Mode
- Protections (OCP: Non-latching, OTP)
- Internal Soft Start
- Compact Size: 6mm*6mm*3.5mm(Max)
- Pb-free for RoHS compliant
- MSL 2, 250°C Reflow

APPLICATIONS:

- Distributed Power Supply
- Server, Workstation, and Storage
- Networking and Datacom

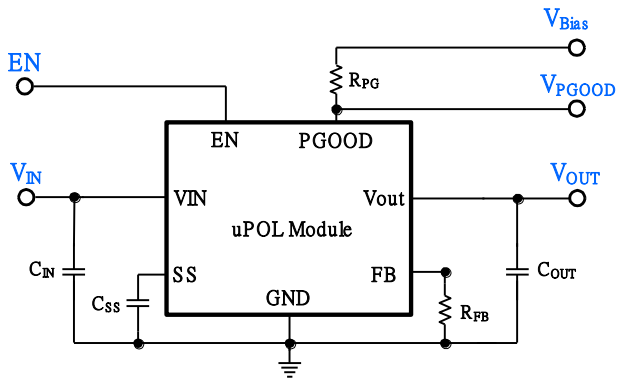
GENERAL DESCRIPTION:

The uPOL module is non-isolated dc-dc converters that can deliver up to 3A of output current. The PWM switching regulator, high frequency power inductor are integrated in one hybrid package. It only needs input/output capacitors and one voltage dividing resistor.

The module has automatic operation with PWM mode and power saving mode according to loading. Other features include remote enable function, internal soft-start, non-latching over current protection and power good.

The low profile and compact size package (6.0mm × 6.0mm x 3.5mm) is suitable for automated assembly by standard surface mount equipment. The uPOL module is Pb-free and RoHS compliance.

TYPICAL APPLICATION CIRCUIT & PACKAGE SIZE:



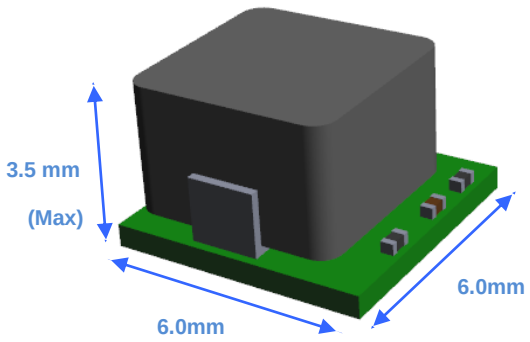


TABLE 1: OUTPUT VOLTAGE SETTING

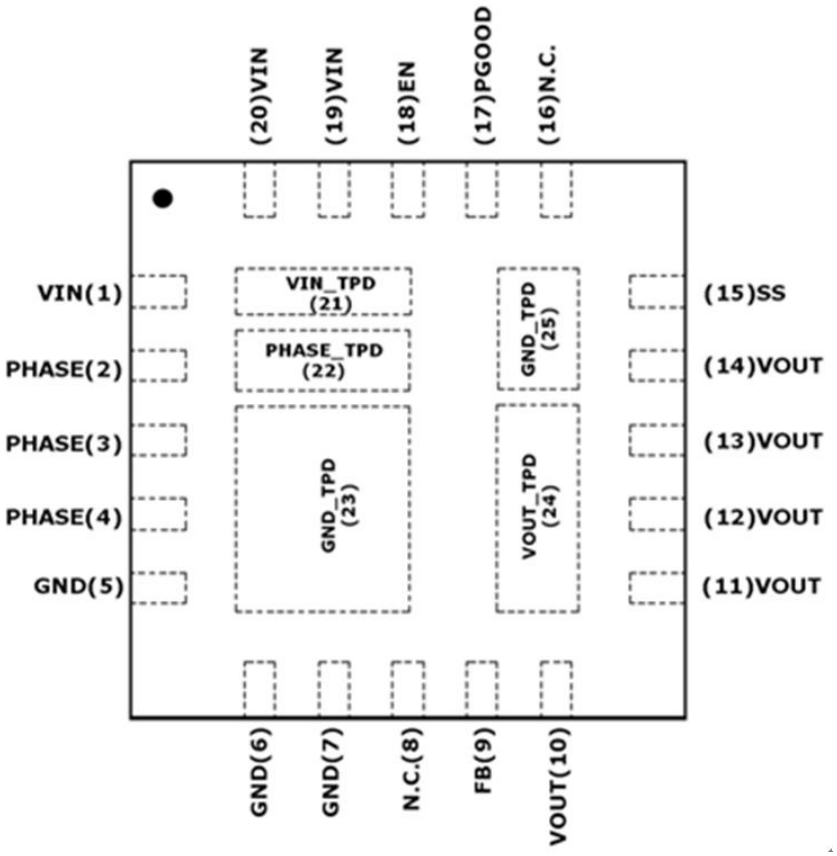
Vout	1.0V	1.2V	1.8V	2.5V	3.3V	5.0V
RFB (Ohm)	150k	100k	49.9k	31.6k	22.1k	13.7k

ORDER INFORMATION:

Part Number	Operating Temperature Range (°C)	Package (Pb-Free)	MSL	Note
MUN12AD03-SM	-40 ~ +125	QFN	Level 2	-

Order Code	Packing	Quantity
MUN12AD03-SM	Tape and reel	1000

PIN CONFIGURATION:



TOP VIEW

PIN DESCRIPTION:

Symbol	Pin No.	Description
VIN	1, 19, 20	Power input pin. It needs to connect input rail and thermal exposed pad of VIN_TPD(21) for heat transferring. Place the input ceramic type capacitor as closely as possible to this pin. One capacitor of 22uF at least for input capacitance.
PHASE	2, 3, 4	Switch output. Connect to thermal exposed pad of PHASE_TPD(22) for heat transferring.
GND	5, 6, 7	Power ground pin for signal, input, and output return path. This pin needs to connect one or more ground plane directly. Connect to thermal exposed pad of GND_TPD(23, 25) for heat transferring.
FB	9	Feedback input. Connect an external resistor divider from the FB to GND to set the output voltage.
VOUT	10, 11, 12, 13, 14	Power output pin. Connect to output and thermal exposed pad of VOUT_TPD(24) for heat transferring. Place the output capacitors as closely as possible to this pin. Two capacitors of 47uF at least for output capacitance.
SS	15	Soft start pin. It has internal current source for changing ramp up to set soft start time. Leave SS pin floating for default 1ms soft-start time.
N.C.	8,16	Not Connected.
PGOOD	17	Power good signal pin. Open drain output when the output voltage is above 90% of regulation point.
EN	18	On/Off control pin for module.
VIN_TPD	21	Power input pin. Connect input rail and using for heat transferring to heat dissipation layer by Vias connection.
PHASE_TPD	22	Phase node pin. Using for heat transferring to heat dissipation layer by Vias connection.
GND_TPD	23, 25	Power ground pin. It needs to connect one or more ground plane directly and using for heat transferring to heat dissipation layer by Vias connection.
VOUT_TPD	24	Power output pin. Connect to output and using for heat transferring to heat dissipation layer by Vias connection.

ELECTRICAL SPECIFICATIONS:

CAUTION: Do not operate at or near absolute maximum rating listed for extended periods of time. This stress may adversely impact product reliability and result in failures not covered by warranty.

Parameter	Description	Min.	Typ.	Max.	Unit
■ Absolute Maximum Ratings					
VIN to GND		-	-	+18	V
VOUT to GND		-	-	+6.5	V
EN to GND		-	-	VIN+0.3	V
Tc	Case Temperature of Inductor	-	-	+110	°C
Tj	Junction Temperature	-40	-	+150	°C
Tstg	Storage Temperature	-40	-	+125	°C
■ Recommendation Operating Ratings					
VIN	Input Supply Voltage	+4.5	-	+16	V
VOUT	Adjusted Output Voltage	+0.6	-	+5.0	V
PGOOD	Power Good Voltage	-	-	+16.0	V
V_{ENH}	EN Rising Threshold	1.5	-	-	V
V_{ENL}	EN Falling Threshold	-	-	0.4	V
Ta	Operating Temperature Range (Note 2)	-40	-	+125	°C
■ Thermal Information					
Rth(j_{choke}-a)	Thermal resistance from junction to ambient (Note 1)	-	14	-	°C/W

NOTES:
1. Rth(j_{choke}-a) is measured with the component mounted on an effective thermal conductivity test board on 0 LFM condition. The test board size is 30mm×30mm×1.6mm with 4 layers. The test condition is complied with JEDEC EIJ/JESD 51 Standards.
2. For maximum operating temperature, thermal derating to be considered.

ELECTRICAL SPECIFICATIONS: (Cont.)

Conditions: T_A = 25 ºC, unless otherwise specified. Test Board Information: 30mm×30mm×1.6mm, 4 layers, 1oz. The output ripple and transient response are measured by short loop probing and limited to 20MHz bandwidth. Cin = 22uF/16V/1206*2, Cout = 47uF/6.3V/1206*2.

Symbol	Parameter	Conditions	Min.	Typ.	Max.	Unit
■ Input Characteristics						
$I_{SD(IN)}$	Input shutdown current	Vin =12V, EN = GND	-	5.5	-	uA
$I_{S(IN)}$	Input supply current	Vin = 12V, EN = VIN	-	-	-	-
		Iout = 0A, Vout = 5.0V	-	0.13	-	mA
		Iout = 5mA,Vout =5.0V	-	2.5	-	mA
		Iout = 3A,Vout =5.0V	-	1.39	-	A
■ Output Characteristics						
$I_{OUT(DC)}$	Output continuous current range		0	-	3	A
$V_{O(SET)}$	Ouput Voltage Set Point	With 0.5% tolerance for external resistor used to set output voltage	-2.5	-	+2.5	% $V_{O(SET)}$
$\Delta V_{OUT}/\Delta V_{IN}$	Line regulation accuracy	Vin = 7.0V to 15V Vout = 5.0V, Iout = 0A Vout = 5.0V, Iout = 3A	-	0.2	-	% $V_{O(SET)}$
$\Delta V_{OUT}/\Delta I_{OUT}$	Load regulation accuracy	Iout = 0A to 3A Vin = 12V, Vout = 5.0V	-2	-	+3	% $V_{O(SET)}$
$V_{OUT(AC)}$	Output ripple voltage	Vin = 12V, Vout = 5.0V EN = VIN,20MHz Bandwidth	-	-	-	-
		IOUT = 5mA	-	25	-	mVp-p
		IOUT = 3A	-	30	-	mVp-p
■ Dynamic Characteristics						
ΔV_{OUT-DP}	Voltage change for positive load step	Iout = 1.5 A to 3A Current slew rate = 0.15A/uS Vin = 12V, Vout = 5V	-	110	-	mVp-p
ΔV_{OUT-DN}	Voltage change for negative load step	Iout = 3A to 1.5A Current slew rate = 0.15A/uS Vin = 12V, Vout = 5V	-	110	-	mVp-p
■ Control Characteristics						
OCP	Protection Output Current		3.8	-	5.2	A
F_{OSC}	Oscillator frequency		-	1	-	MHz
V_{REF}	Referance voltage		-1.5	0.600	+1.5	V/%
V_{PG}	Power good threshold		88	90	92	% V_{REF}
V_{PGL}	PGOOD output low	I_{PGOOD}=4mA	0.04	0.15	0.3	V
$Toff_{MIN}$	Minimum Off time		140	170	220	nS
Ton_{MIN}	Minimum On time		50	80	120	nS

TYPICAL PERFORMANCE CHARACTERISTICS: (1.0VOUT)

Conditions: T_A = 25 ºC, unless otherwise specified. Test Board Information: 30mm×30mm×1.6mm, 4 layers, 1oz.
The output ripple and transient response are measured by short loop probing and limited to 20MHz bandwidth.
Cin = 22uF/16V/1206*2, Cout = 47uF/6.3V/1206*2.
The following figures are the typical characteristic curves at 1.0Vout.

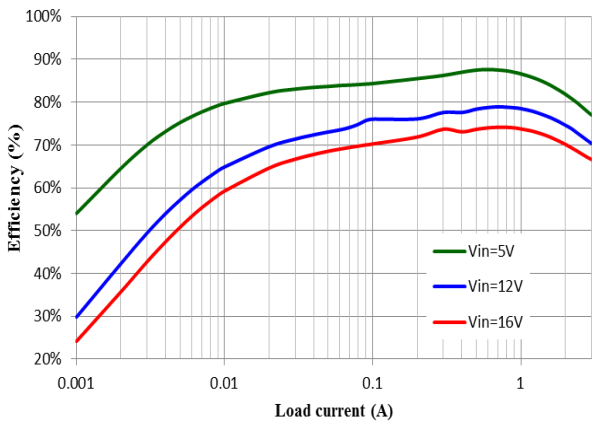


FIG.1 Efficiency V.S. Load Current

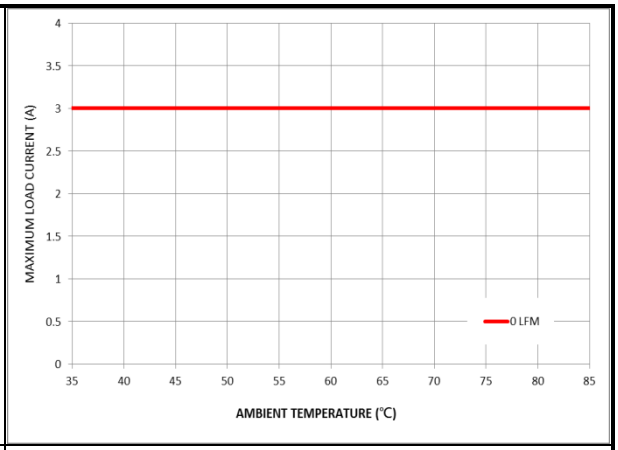


FIG.2 De-rating Curve at 12Vin

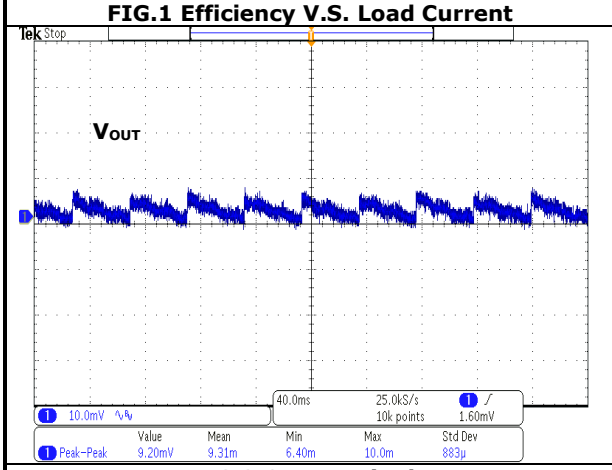


FIG.3 Output Ripple (12Vin, Iout=0A)

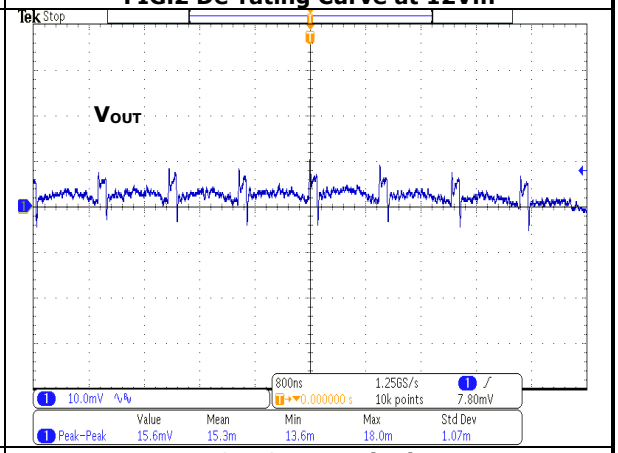


FIG.4 Output Ripple (12Vin, Iout=3A)

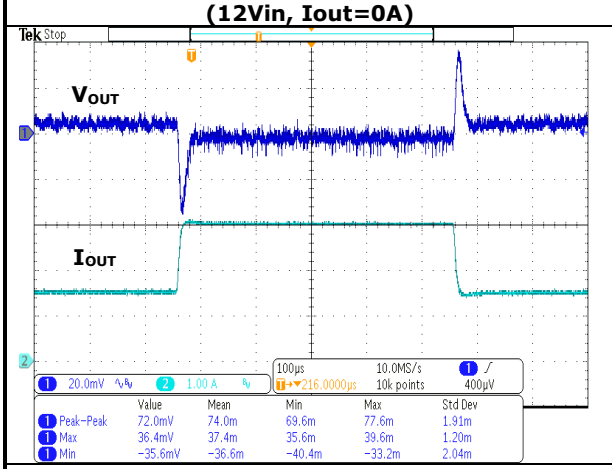


FIG.5 TRANSIENT RESPONSE (12VIN, 50% to 100% LOAD STEP)

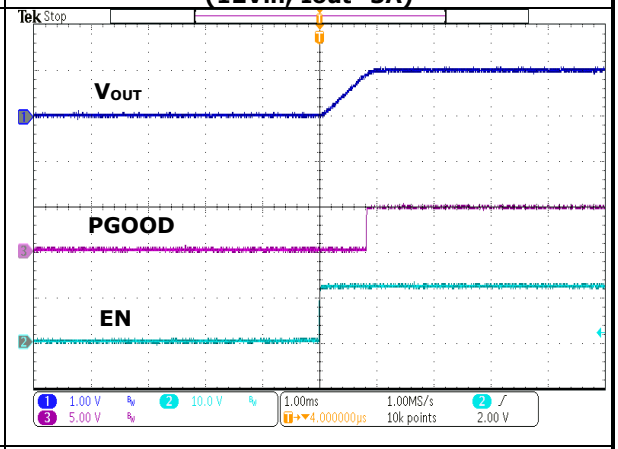


FIG.6 Turn-on (12Vin, Iout=3A)

TYPICAL PERFORMANCE CHARACTERISTICS: (1.8VOUT)

Conditions: T_A = 25 ºC, unless otherwise specified. Test Board Information: 30mm×30mm×1.6mm, 4 layers, 1oz.
The output ripple and transient response are measured by short loop probing and limited to 20MHz bandwidth.
Cin = 22uF/16V/1206*2, Cout = 47uF/6.3V/1206*2.
The following figures are the typical characteristic curves at 1.8Vout.

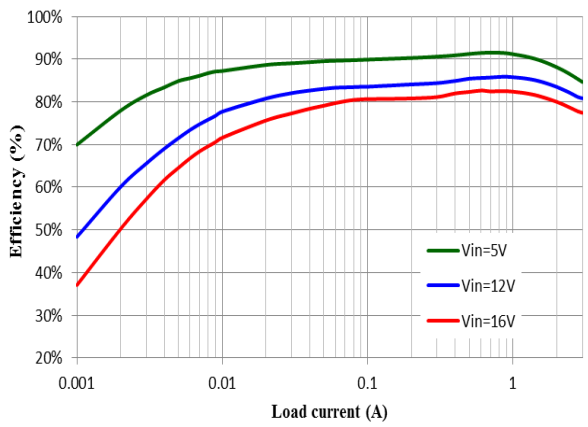


FIG.7 Efficiency V.S. Load Current

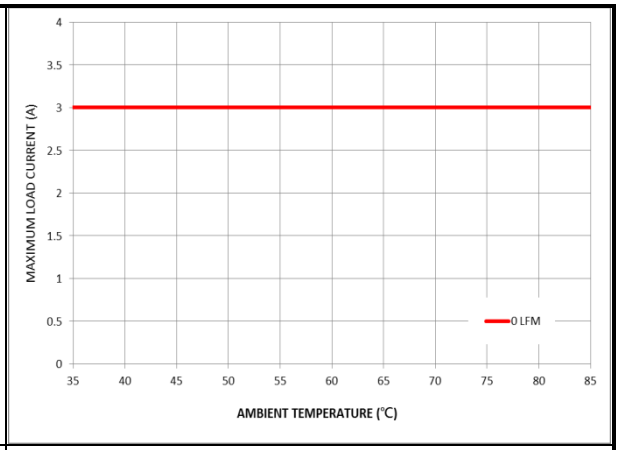


FIG.8 De-rating Curve at 12Vin

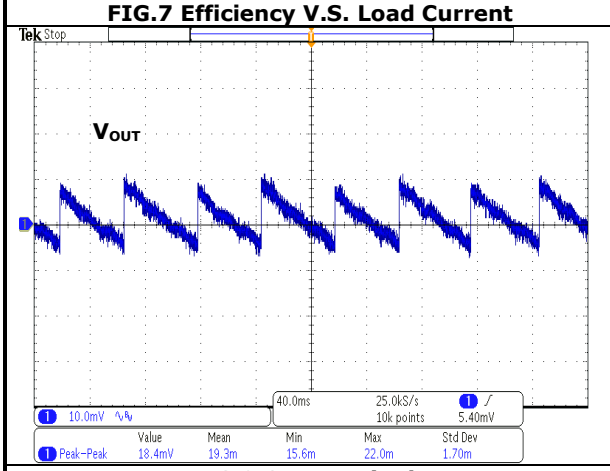


FIG.9 Output Ripple
(12Vin, Iout=0A)

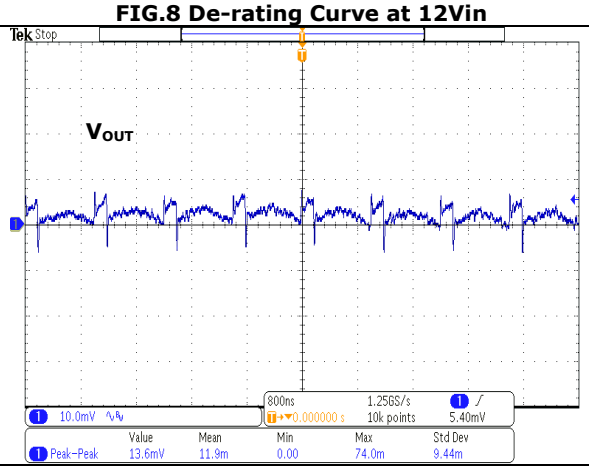


FIG.10 Output Ripple
(12Vin, Iout=3A)

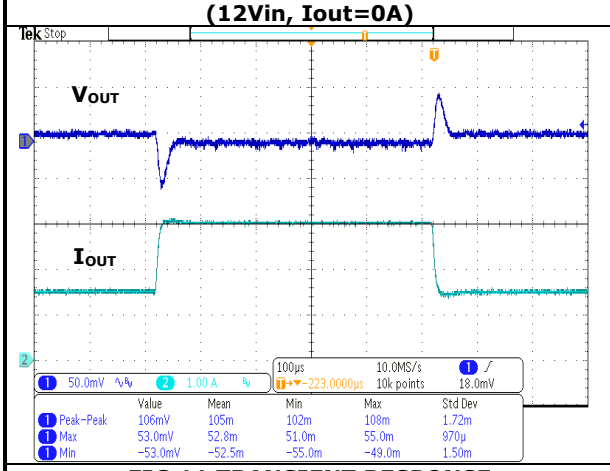


FIG.11 TRANSIENT RESPONSE
(12VIN, 0% to 100% LOAD STEP)

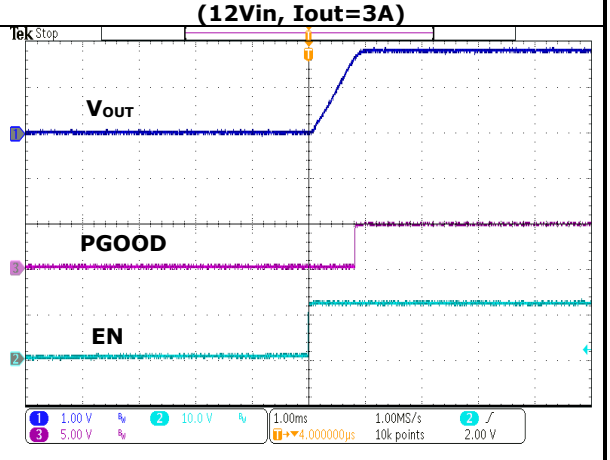


FIG.12 Turn-on
(12Vin, Iout=3A)

TYPICAL PERFORMANCE CHARACTERISTICS: (3.3VOUT)

Conditions: T_A = 25 ºC, unless otherwise specified. Test Board Information: 30mm×30mm×1.6mm, 4 layers, 1oz.
The output ripple and transient response are measured by short loop probing and limited to 20MHz bandwidth.
Cin = 22uF/16V/1206*2, Cout = 47uF/6.3V/1206*2.
The following figures are the typical characteristic curves at 3.3Vout.

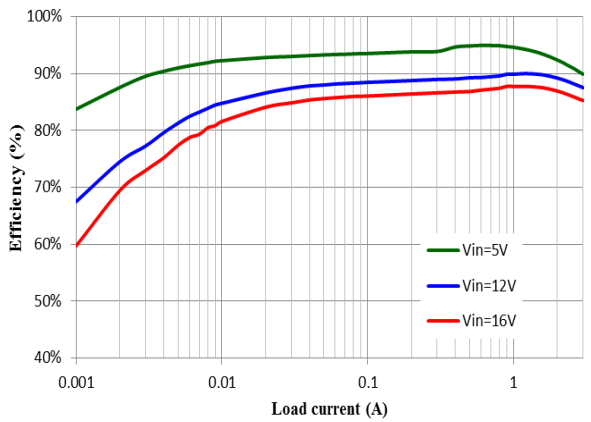


FIG.13 Efficiency V.S. Load Current

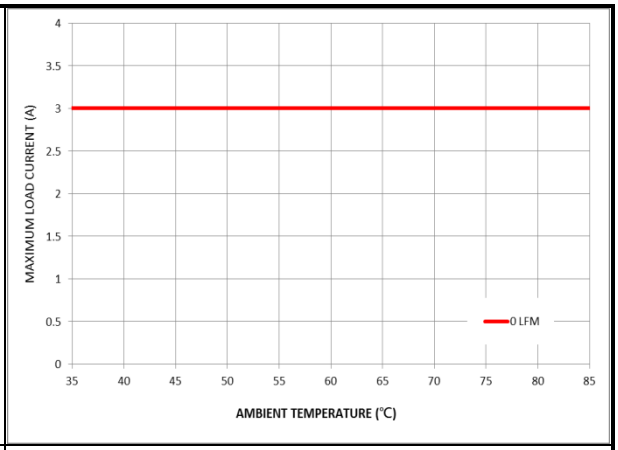


FIG.14 De-rating Curve at 12Vin

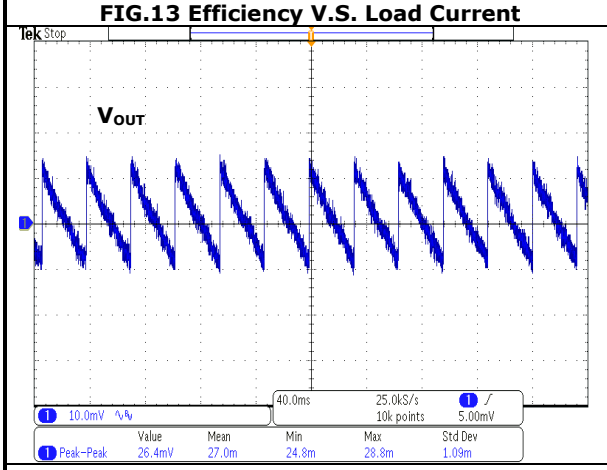


FIG.15 OUTPUT RIPPLE (12VIN, IOUT=0A)

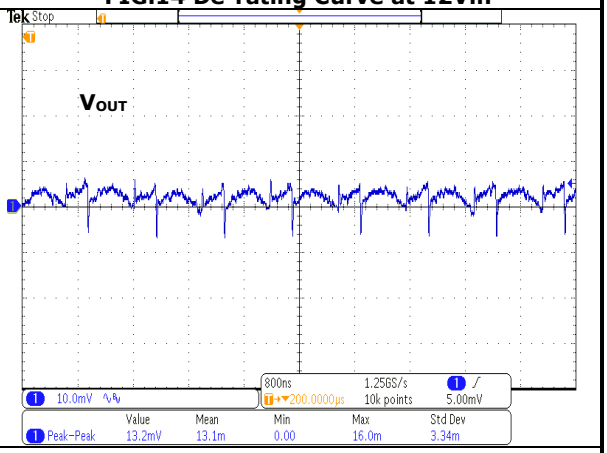


FIG.16 OUTPUT RIPPLE (12VIN, IOUT=3A)

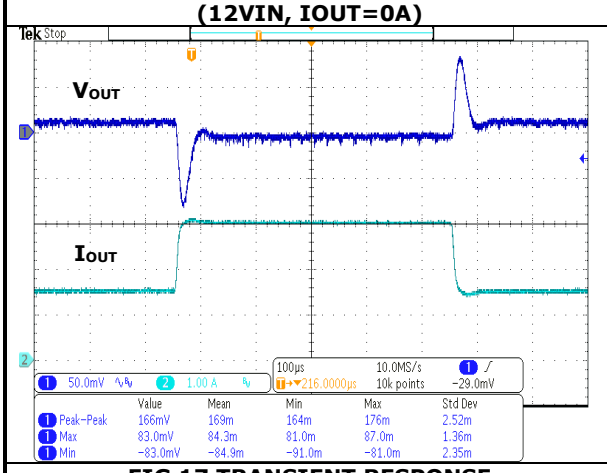


FIG.17 TRANSIENT RESPONSE (12VIN, 50% to 100% LOAD STEP)

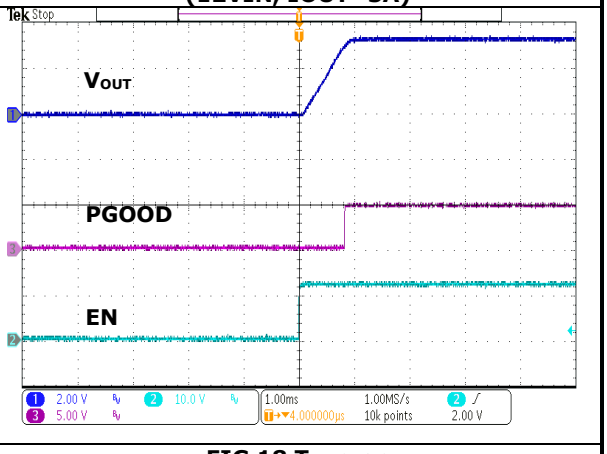


FIG.18 Turn-on (12Vin, Iout=3A)

TYPICAL PERFORMANCE CHARACTERISTICS: (5.0VOUT)

Conditions: T_A = 25 ºC, unless otherwise specified. Test Board Information: 30mm×30mm×1.6mm, 4 layers, 1oz.
The output ripple and transient response are measured by short loop probing and limited to 20MHz bandwidth.
Cin = 22uF/16V/1206*2, Cout = 47uF/6.3V/1206*2.
The following figures are the typical characteristic curves at 5.0Vout.

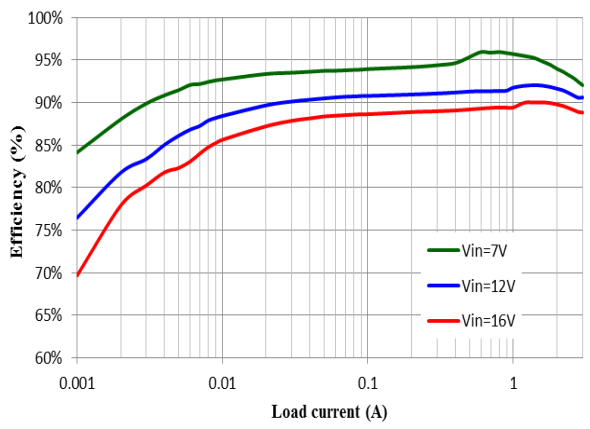


FIG.19 Efficiency V.S. Load Current

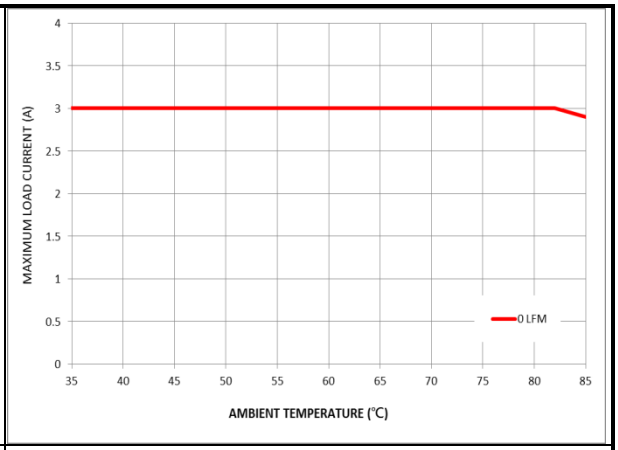


FIG.20 De-rating Curve at 12Vin

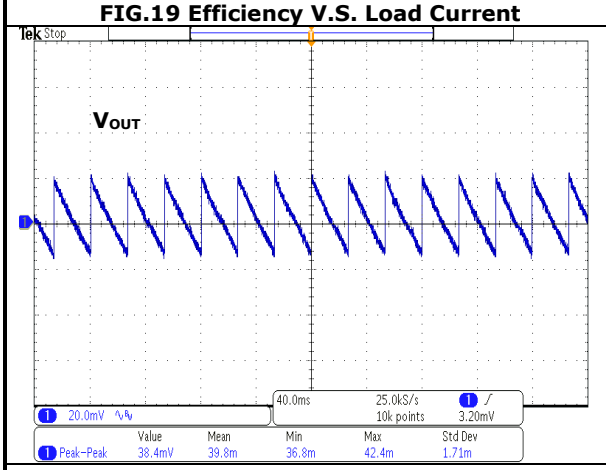


FIG.21 OUTPUT RIPPLE
(12VIN, IOUT=0A)

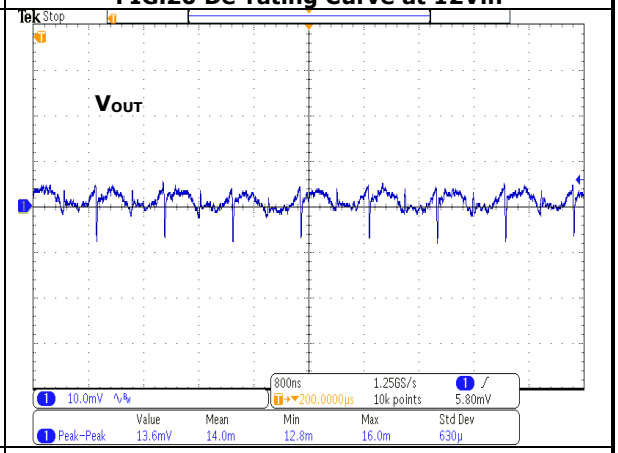


FIG.22 OUTPUT RIPPLE
(12VIN, IOUT=3A)

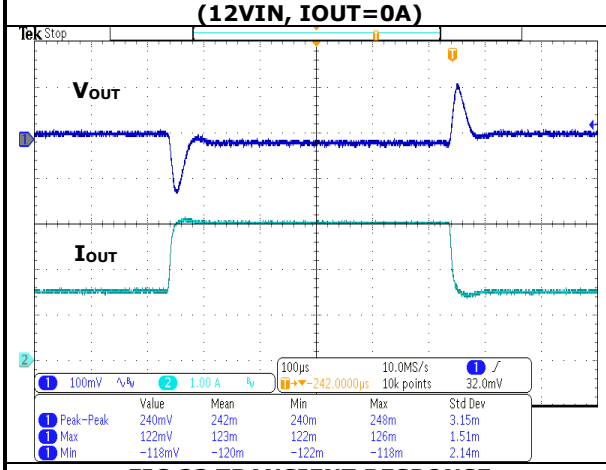


FIG.23 TRANSIENT RESPONSE
(12VIN, 50% to 100% LOAD STEP)

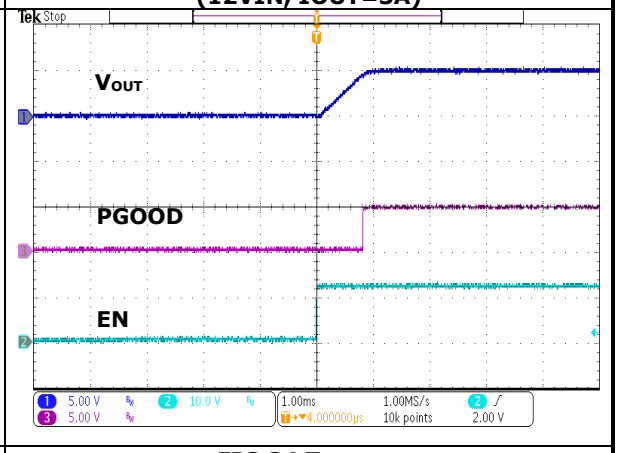


FIG.24 Turn-on
(12Vin, Iout=3A)

APPLICATIONS INFORMATION:

REFERENCE CIRCUIT FOR GENERAL APPLICATION:

The Figure 25 shows the MUN12AD03-SM application schematics for input voltage +12V with automatic power saving function operation.

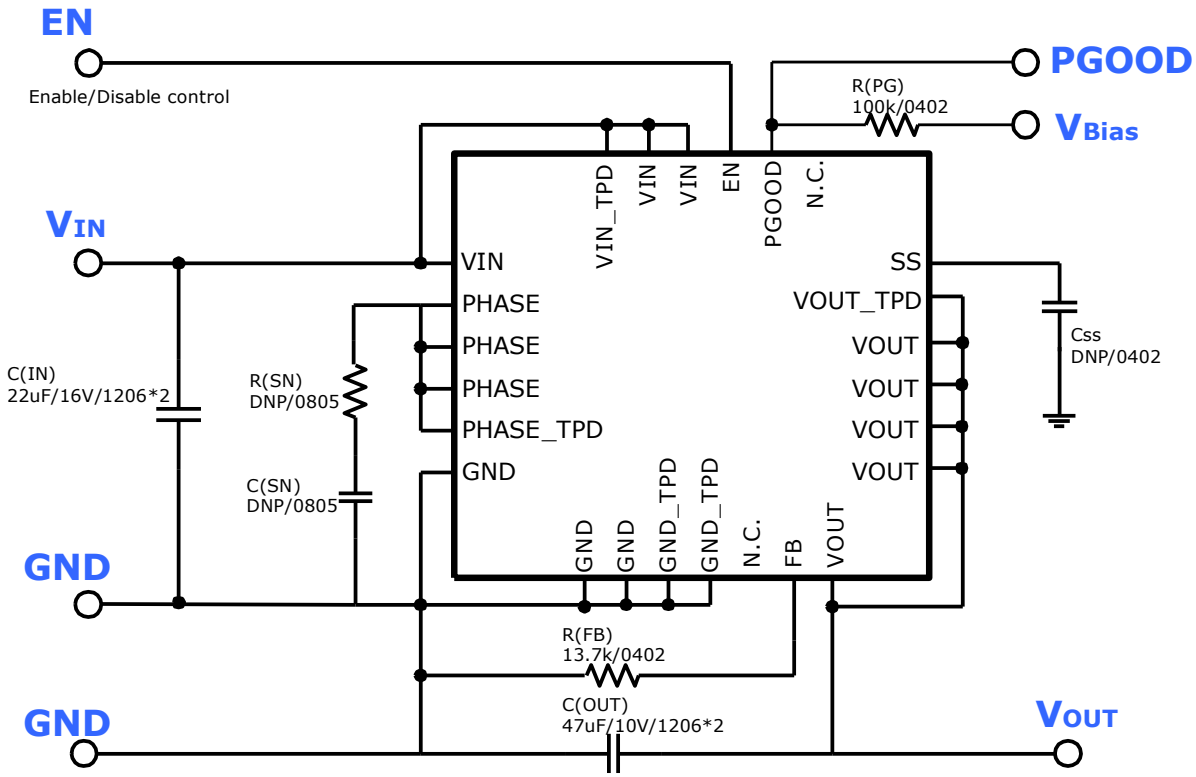


FIG.25 TYPICAL APPLICATION FOR PWM OPERATION

APPLICATIONS INFORMATION: (Cont.)

SAFETY CONSIDERATIONS:

Certain applications and/or safety agencies may require fuses at the inputs of power conversion components. Fuses should also be used when there is the possibility of sustained input voltage reversal which is not current limited. For greatest safety, we recommend a fast blow fuse installed in the ungrounded input supply line. The installer must observe all relevant safety standards and regulations. For safety agency approvals, install the converter in compliance with the end-user safety standard.

INPUT FILTERING:

The module should be connected to as low AC impedance source supply and a highly inductive source or line inductance can affect the stability of the module. Input capacitors must be placed directly to the input pin of the module, to minimize input ripple voltage and ensure module stability.

OUTPUT FILTERING:

To reduce output ripple and improve the dynamic response to as step load change, the additional capacitors at the output must be used. Low ESR polymer and ceramic capacitors are recommended to improve the output ripple and dynamic response of the module.

PROGRAMMING OUTPUT VOLTAGE:

The module has an internal 0.6V±1.5% reference voltage. The output voltage can be programmed by the dividing resistance R_{FB} which respects to FB pin and GND pin. The output voltage can be calculated as shown in Equation 1 and the resistance according to typical output voltage is shown in TABLE 1.

$$\mathrm{VOUT\ (V)} = 0.6 \times \left(1 + \frac{100\mathrm{k}}{\mathrm{R_{FB}}}\right) \qquad \text{(EQ.1)}$$

PROGRAMMING SOFT-START:

Leave SS pin float for default 1ms soft-start time. This mechanism provides output voltage soft rise and no inrush current charges the output capacitors. The soft start time can be calculated as shown in Equation 2 for reference.

$$T_{SS}\,(Sec) = \frac{C_{ss} \times 0.6V}{4uA} \qquad \text{(EQ.2)}$$

APPLICATIONS INFORMATION: (Cont.)

RECOMMENDATION LAYOUT GUIDE:

In order to achieve stable, low losses, less noise or spike, and good thermal performance some layout considerations are necessary. The recommendation layout is shown as Figure 26.

1. The ground connection between pin 23, pin25 and pin 5 to 7 should be a solid ground plane under the module. It can be connected one or more ground plane by using several Vias.
2. Place high frequency ceramic capacitors between pin 1, pin 19 to 21 (VIN), and pin 23, pin25, pin 5 to 7 (GND) for input side; and pin 24, pin 10 to 14 (VOUT), and pin 23, pin25, pin 5 to 7 (GND) for output side, as close to module as possible to minimize high frequency noise.
3. Keep the R_{FB} connection trace to the module pin 9 (FB) short.
4. Use large copper area for power path (VIN, VOUT, and GND) to minimize the conduction loss and enhance heat transferring. Also, use multiple Vias to connect power planes in different layer.
5. Avoid any sensitive signal traces near the pin 24, and pin 2 to 4 (PHASE).

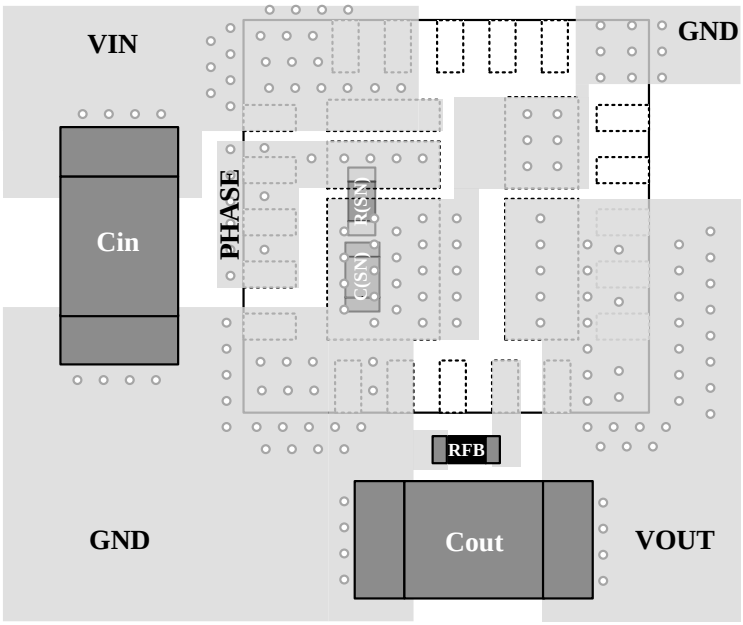


FIG.26 RECOMMENDATION LAYOUT (TOP LAYER)

APPLICATIONS INFORMATION: (Cont.)

Thermal Considerations:

All of thermal testing condition is complied with JEDEC EIJ/JESD 51 Standards. Therefore, the test board size is 30mm×30mm×1.6mm with 4 layers. The case temperature of module sensing point is shown as Figure 27. Then Rth(j_{choke}-a) is measured with the component mounted on an effective thermal conductivity test board on 0 LFM condition. The MUN12AD03-SM module is designed for using when the case temperature is below 110°C regardless the change of output current, input/output voltage or ambient temperature.

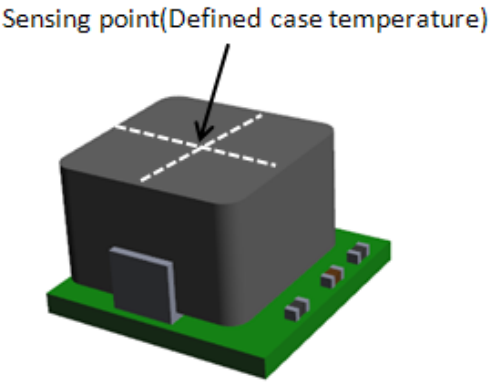


Figure 27 Case Temperature Sensing Point

REFLOW PARAMETERS:

Lead-free soldering process is a standard of electronic products production. Solder alloys like Sn/Ag, Sn/Ag/Cu and Sn/Ag/Bi are used extensively to replace the traditional Sn/Pb alloy. Sn/Ag/Cu alloy (SAC) is recommended for this power module process. In the SAC alloy series, SAC305 is a very popular solder alloy containing 3% Ag and 0.5% Cu and easy to obtain. Figure 28 shows an example of the reflow profile diagram. Typically, the profile has three stages. During the initial stage from room temperature to 150°C, the ramp rate of temperature should not be more than 3°C/sec. The soak zone then occurs from 150°C to 200°C and should last for 60 to 120 seconds. Finally, keep at over 217°C for 60 seconds limit to melt the solder and make the peak temperature at the range from 240°C to 250°C. It is noted that the time of peak temperature should depend on the mass of the PCB board. The reflow profile is usually supported by the solder vendor and one should adopt it for optimization according to various solder type and various manufacturers' formulae.

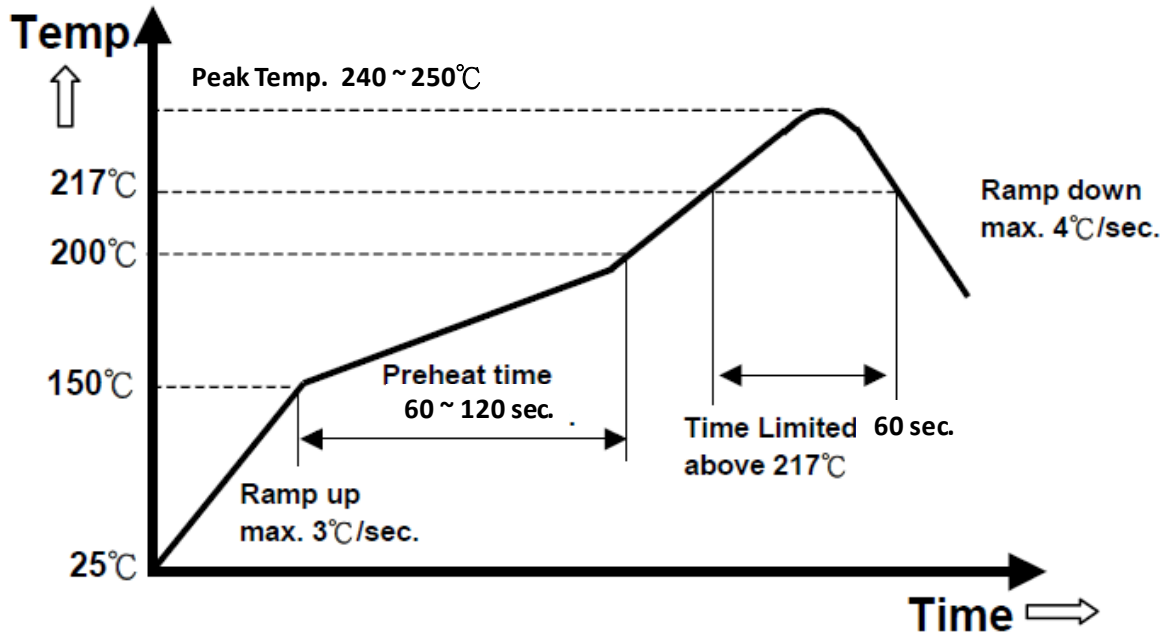
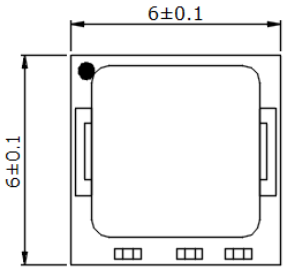


FIG.28 Recommendation Reflow Profile

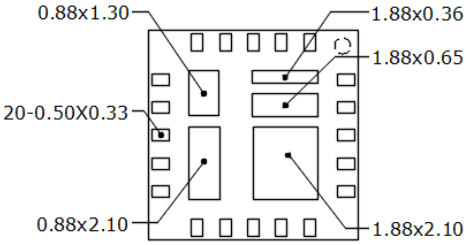
PACKAGE OUTLINE DRAWING:

unit: mm

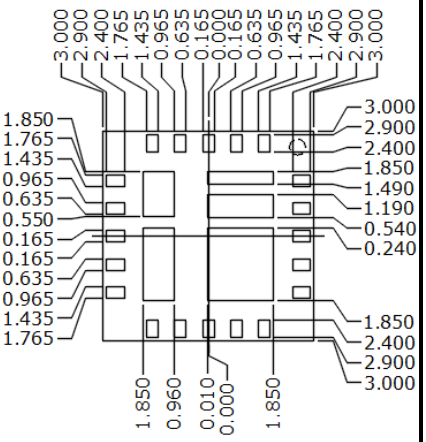
General Tolerance: ±0.1mm



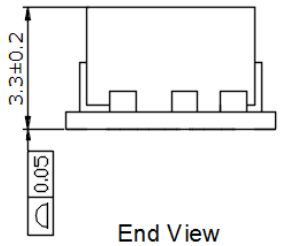
Top View



Bottom View



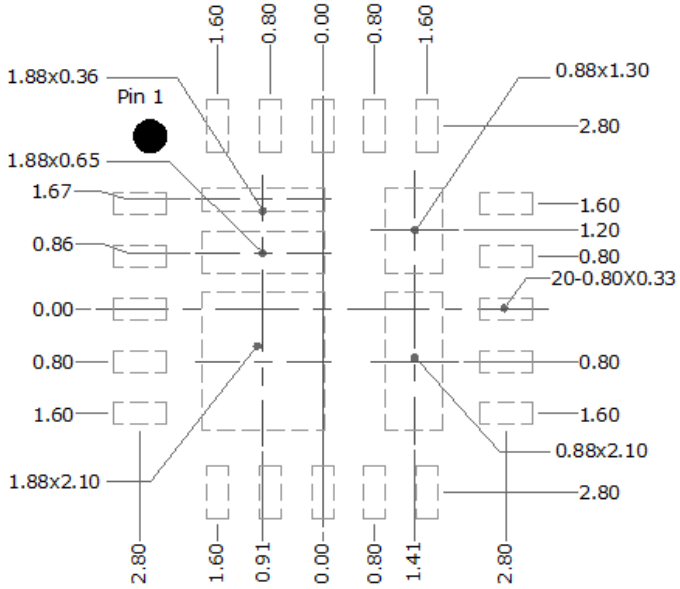
Bottom View



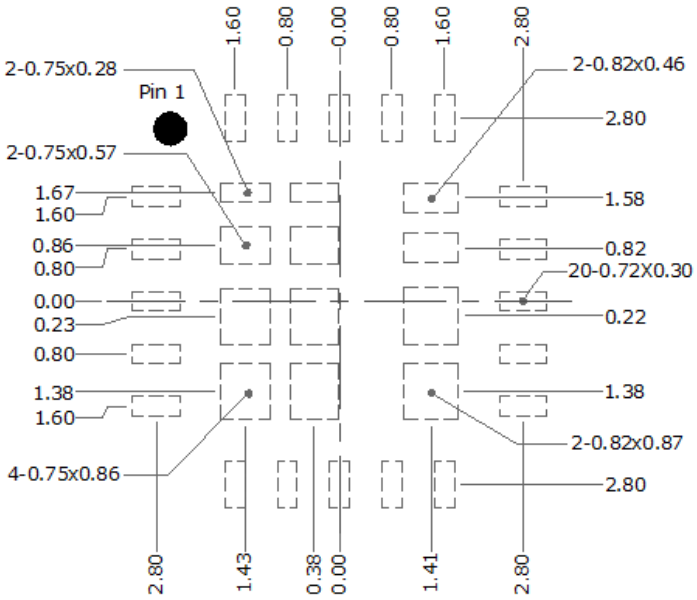
End View

LAND PATTERN REFERENCE:

Unit:mm



TYPICAL RECOMMENDED LAND PATTERN

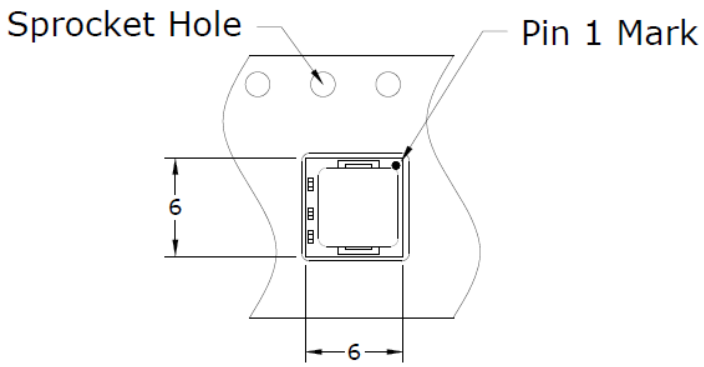


RECOMMENDED STENCIL PATTERN
BASED ON 0.1mm THICKNESS STENCIL

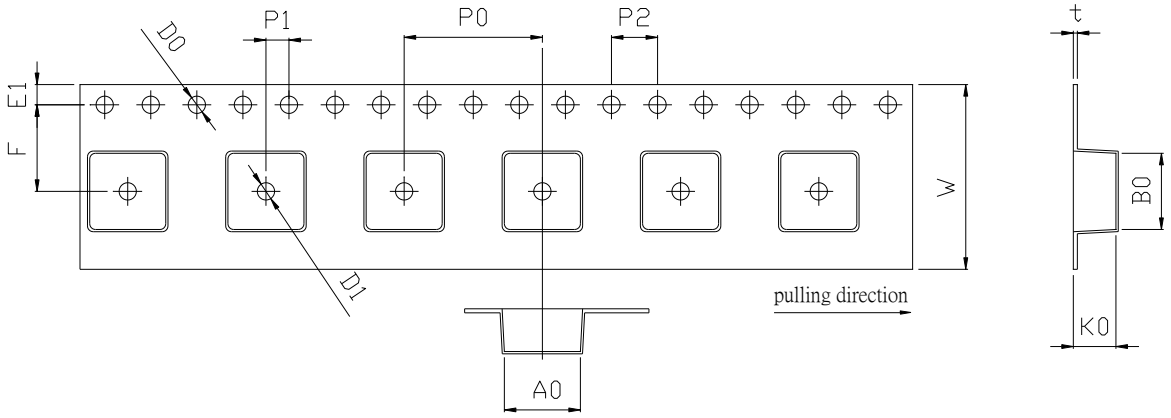
PACKING REFERENCE:

Unit: mm

Package In Tape Loading Orientation



Tape Dimension

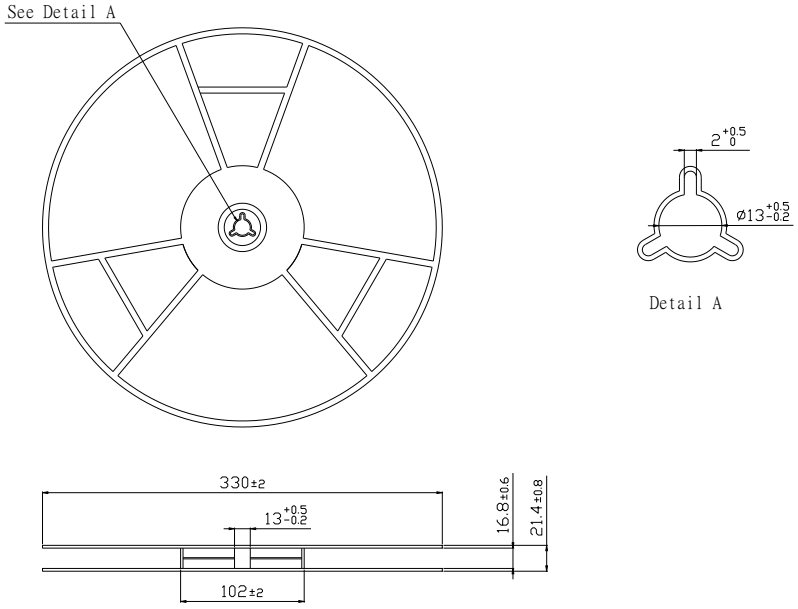


A0	6.60 ± 0.10	E1	1.75 ± 0.10
B0	6.60 ± 0.10	K0	3.70 ± 0.10
F	7.50 ± 0.10	P0	12.00 ± 0.10
W	16.00 ± 0.30	P1	2.00 ± 0.10
D0	φ1.5 +0.1/-0.0	P2	4.00 ± 0.10
D1	φ1.5 Min.	t	0.35 ± 0.05

PACKING REFERENCE: (Cont.)

Unit: mm

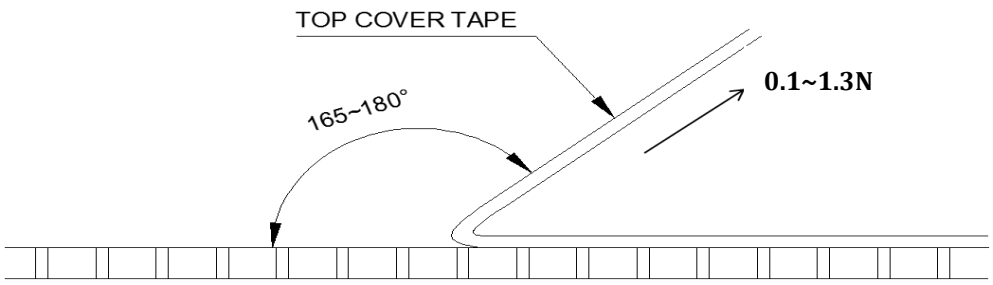
Reel Dimension



Peel Strength of Top Cover Tape

The peel speed shall be about 300mm/min.

The peel force of top cover tape shall between 0.1N to 1.3N



REVISION HISTORY:

Date	Revision	Changes
2014.11.20	00	Release the preliminary specification.
2014.12.18	01	Add packing and marking drawing.
2015.02.12	02	Change PIN 1 position: PIN CONFIGURATION, PACKAGE OUTLINE DRAWING, LAND PATTERN REFERENCE, PACKING REFERENCE
2015.02.26	03	1. Thermal Information: ● Delete Note 2 test board oz
2015.05.07	04	Change $I_{SD(IN)}$ and $I_{Q(IN)}$ current
2015.06.10	05	Change Recommendation Vout Operating Ratings
2015.06.24	06	Add REFLOW PARAMETERS
2015.10.28	07	Change MSL level
2015.11.13	08	Change recommendation reflow profile
2016.06.28	09	Modify land pattern reference
2016.09.08	10	Change MSL level: MSL 3 → MSL 2
2017.03.24	11	Add PGOOD sink current spec
2024.12.16	A1	Redefine version