High Efficiency DC/DC Power Module

MSN24VD03-GR

FEATURES:

- High Density Power Module
- 3A Output Current
- Input Voltage Range from 5.1V to 24V
- Selectable 5.1V, 6V, 7V, 8V, 9V, 12V, 15V, 20V Output Voltage (Note 1)
- 94% Peak Efficiency
- 100% Duty-Cycle Operation
- Output Line-drop Compensation
- Protections (OCP, OTP, OVP, UVP, Non-latching)
- LGA Package (9.4 X 8.6 X 6.3mm max)
- Pb-free Available (RoHS compliant)
- MSL 3, 245°C Reflow

APPLICATIONS:

- Power Supply for Linear Charge
- USB Power Supply

GENERAL DESCRIPTION:

The MSN24VD03-GR is a high frequency, high power density and complete DC/DC power module. The PWM controller, power MOSFETs and most of support components are integrated into one hybrid package.

It uses constant on-time control scheme to handle wide input/ output voltage ratios with ease and provides fast "instant-on" response to load transients while maintaining a relatively constant switching frequency. MSN24VD03-GR is with single-stage buck conversion allows these devices to directly step down high-voltage input for the highest possible efficiency.

MSN24VD03-GR is with programmable output voltage by VID pins and supports USB Power Delivery (PD) requirement

TYPICAL APPLICATION CIRCUIT & PACKAGE SIZE:

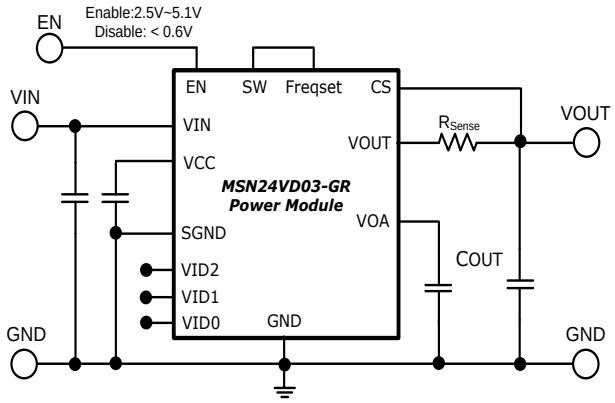


FIG.1 Typical Application Circuit

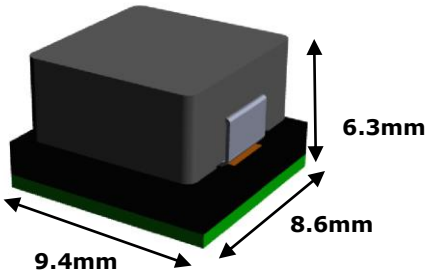


FIG.2 High Density Power Module

VID2	VID1	VID0	Output Voltage
0	0	0	5.1V
0	0	1	6V
0	1	0	7V
0	1	1	8V
1	0	0	9V
1	0	1	12V
1	1	0	15V
1	1	1	20V

Table 1: Output Voltage Setting (Note 1)

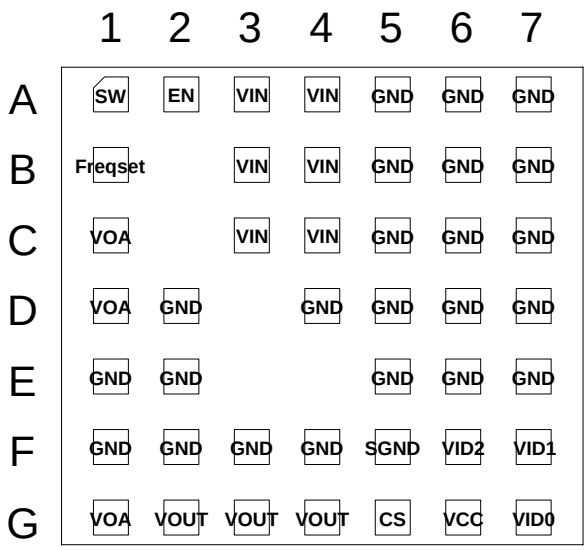
ORDER INFORMATION:

Part Number	Ambient Temp. Range (°C)	Package (Pb-Free)	MSL	Note
MSN24VD03-GR	-40 ~ +85	LGA	Level 3	-

Order Code	Packing	Quantity
MSN24VD03-GR	Tray	800

- This product is not recommended for second (back) side reflow.

PIN CONFIGURATION:



Top View

Symbol	Pin No.	Description
SW	A1,	Switching node pin.
Freqset	B1	Switching frequency define pin. It has an integrated internal 412kΩ resistor. The Freqset pin needs to be short with SW pin; Default switching frequency is 500k Hz typical operation.
VIN	A3,A4,B3,B4,C3,C4	Power input pin. Bypass to GND with 22μF (min) Capacitor.

PIN DESCRIPTION: (Cont.)

Symbol	Pin No.	Description
GND	A5-A7,B5-B7,C5-C7,D2,D4-D7, E1-E2,E5-E7,F1-F4	Power ground pin.
SGND	F5	Analog Ground.
VOUT	G2-G4	Power output pin. Connect to output for the load.
VOA	C1,D1,G1	Output Voltage Connection. Connect directly to the junction of external and Output filter capacitors.
CS	G5	Current Sense Pin.
EN	A2	Enable: input 2.5V~5.1V for En pin Disable: to pull the pin lower than 0.6V(typ.) It has an integrated internal 10kΩ resistor to GND pin.
VID0	G7	Output Voltage Selection Pin.
VID1	F7	Output Voltage Selection Pin
VID2	F6	Output Voltage Selection Pin
VCC	G6	5V Linear Regulator Output. Supply for Internal circuits. Bypass to SGND with a 10μF(min) ceramic capacitor.

ELECTRICAL SPECIFICATIONS:

CAUTION: Do not operate at or near absolute maximum rating listed for extended periods of time. This stress may adversely impact product reliability and result in failures not covered by warranty.

Parameter	Description	Min.	Typ.	Max.	Unit
■ Absolute Maximum Ratings					
VIN to SGND		-0.3	-	+28	V
VCC to SGND		-0.3	-	+6.0	V
Freqset to SND		-0.3	-	+6.0	V
VOA,VOUT to GND		-0.3	-	+22	V
EN, to SGND		-0.3	-	+5.5	V
VID0,VID1,VID2 to SGND		-0.3	-	+5.5	V
Tc	Choke temperature	-	-	+110	°C
Tj	Operating temperature	-40	-	+125	°C
Tstg	Storage temperature	-40	-	+125	°C
ESD	Human Body Model (HBM)	-	-	2k	V
	Charge Device Model (CDM)	-	-	500	V
■ Recommendation Operating Ratings					
VIN	Input Supply Voltage	+5.1	-	+24	V
Ta	Ambient Temperature	-40	-	+85	°C
■ Thermal Information					
Rth(ja)	Thermal resistance from junction to ambient. (Note 2)	-	35.2	-	°C/W

NOTES:
1. If output voltage set to 20V, please keep input voltage between 20V to 21V.
2. The test board size is 30mm×30mm×1.6mm with 2 layers 2oz, on 0 LFM condition.
   The test condition is complied with JEDEC EIJ/JESD 51 Standards.

ELECTRICAL SPECIFICATIONS: (Cont.)

Conditions: T_A = 25 ºC, unless otherwise specified. Test Board Information: 30mm×30mm×1.6mm, 2 layers 2Oz .
The output ripple and transient response measurement is short loop probing and 20MHz bandwidth limited.

Vin = 20.0V, Vout = 5.1V, unless otherwise specified.
Cin = 22uF/25V/1210X 2, Cout = 22uF/25V/1210X 2+ ALUM POLY 56uF/25V (ESR:50mΩ)

Symbol	Parameter	Conditions	Min.	Typ.	Max.	Unit
■ Input Characteristics						
I_{IN}	Input supply bias current	Iout = 0A Vin = 20V, Vout = 5.1V	-	0.5	-	mA
I_S	Input supply current	Iout = 3A Vin =20V, Vout = 5.1V	-	0.85	-	A
■ Output Characteristics						
$I_{OUT(DC)}$	Output continuous current range		0	-	3	A
$\Delta V_{OUT}/\Delta V_{IN}$	Line regulation accuracy	Vin = 5.2V to 24V Vout = 5.1V, Iout = 0A	-	1	-	%
$V_{OUT(AC)}$	Output ripple voltage	Iout = 3A Vin = 20V, Vout = 5.1V	-	50	-	mVp-p
■ Control Characteristics						
VID0,VID1,VID2	Logic Input High Voltage		1.4	-	5.1	V
	Logic Input Low Voltage		-	-	0.6	V
EN	EN Input High Voltage		2.5	-	5.1	V
	EN Input Low Voltage		-	-	0.6	V
V_{UVLO}	PWM disabled	hysteresis = 200mV	3.7	-	4.3	V
SS	Soft-Start Ramp Time	Rising edge of VCC>UVLO to 95% output voltage	-	2.5	-	mS
F_{OSC}	Oscillator frequency		-	500	-	kHz
■ Fault Protection						
OVP	Output overvoltage protection		-	115	-	%
UVP	Output undervoltage protection		48	58	68	%
OCP	Over-current threshold		-	4.5	-	A
T_{TSD}	Shutdown temperature		-	152	-	℃

TYPICAL PERFORMANCE CHARACTERISTICS: (5.1 VOUT)

Conditions: TA = 25 ºC, unless otherwise specified. Test Board Information: 30mm×30mm×1.6mm, 2 layers 2Oz. The output ripple and transient response measurement is short loop probing and 20MegHz bandwidth limited. Cin = 22uF/25V/1210X 2, Cout = 22uF/25V/1210X 2+56uF/25V (ESR:50mΩ)

The following figures provide the typical characteristic curves at 5.1Vout.

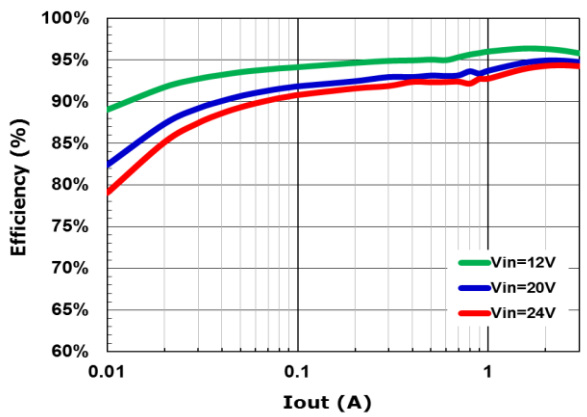


FIG.3 Efficiency V.S. Load Current

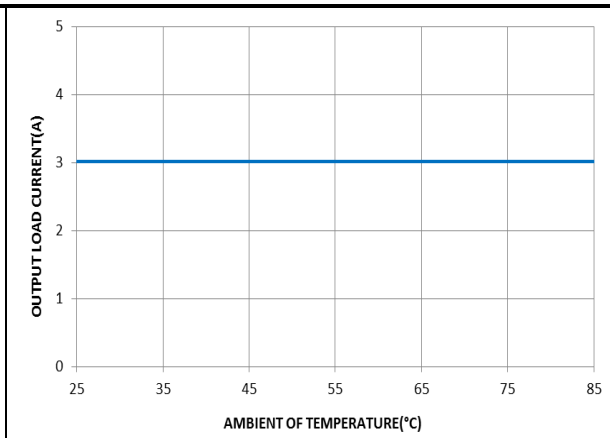


FIG.4 De-rating Curve

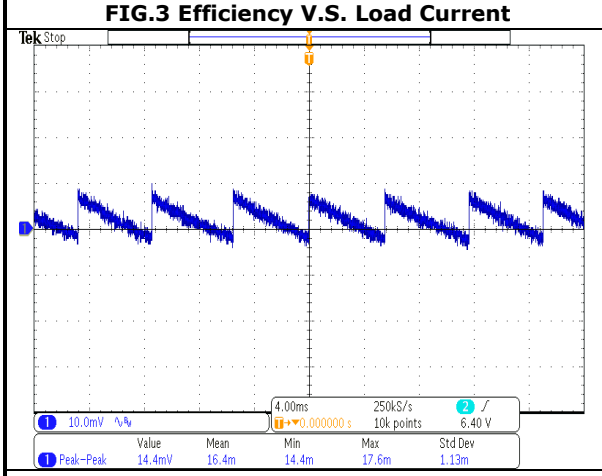


FIG.5 Output Ripple (20Vin, Iout=0A)

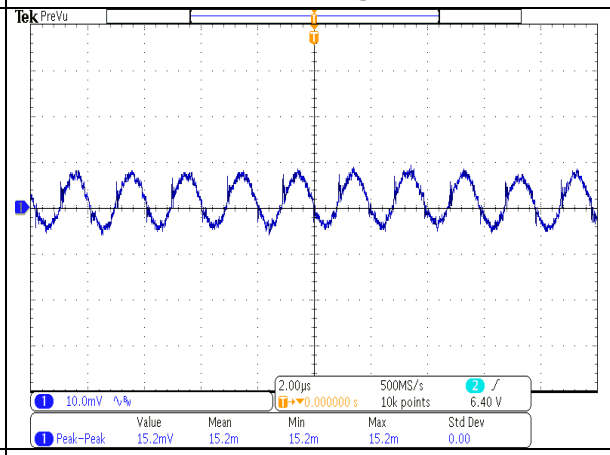


FIG.6 Output Ripple (20Vin, Iout=3A)

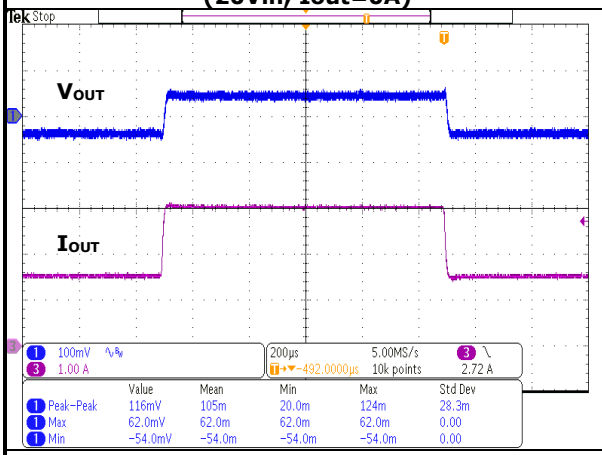


FIG.7 Transient Response (20Vin, 50% to 100% Load Step)

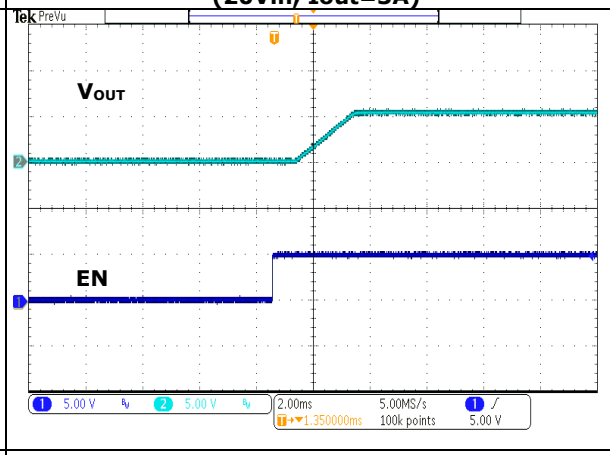


FIG.8 Turn-on (20Vin, Iout=0A)

TYPICAL PERFORMANCE CHARACTERISTICS: (6.0 VOUT)

Conditions: TA = 25 ºC, unless otherwise specified. Test Board Information: 30mm×30mm×1.6mm, 2 layers 2Oz. The output ripple and transient response measurement is short loop probing and 20MegHz bandwidth limited. Cin = 22uF/25V/1210X 2, Cout = 22uF/25V/1210X2 +56uF/25V (ESR:50mΩ)

The following figures provide the typical characteristic curves at 6.0Vout.

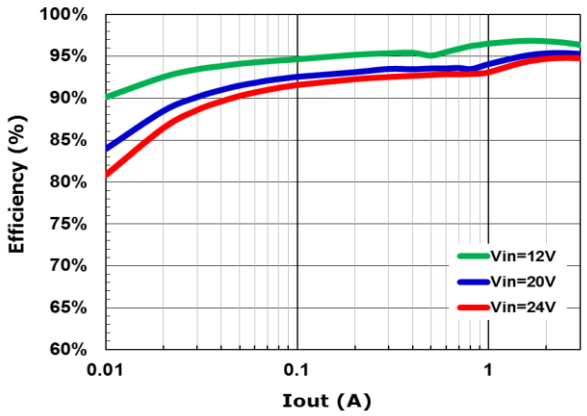


FIG.9 Efficiency V.S. Load Current

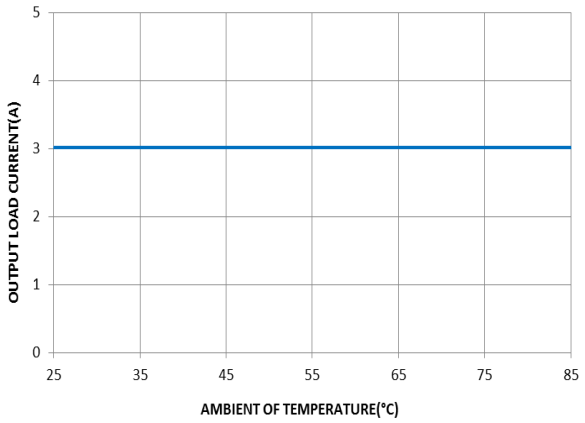


FIG.10 De-rating Curve

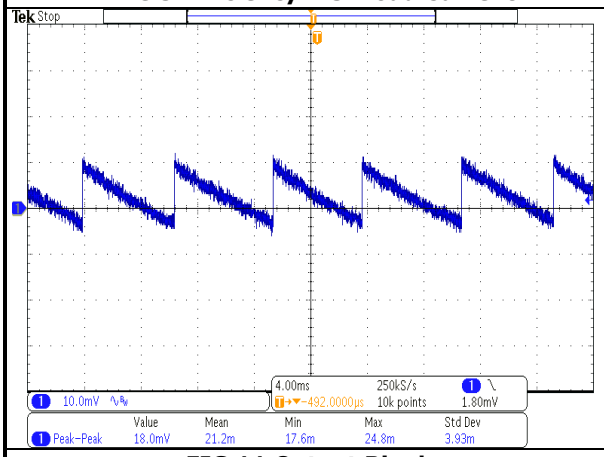


FIG.11 Output Ripple (20Vin, Iout=0A)

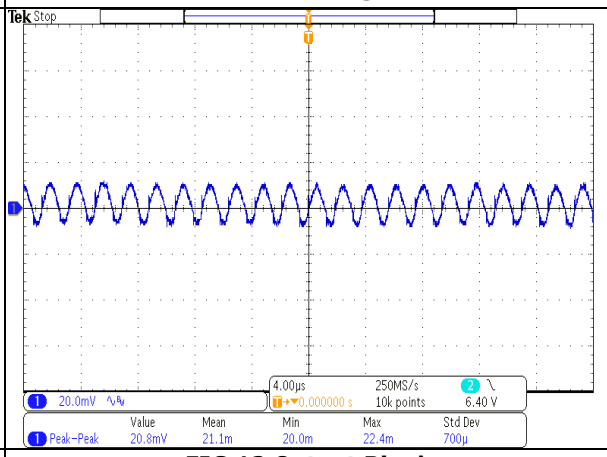


FIG.12 Output Ripple (20Vin, Iout=3A)

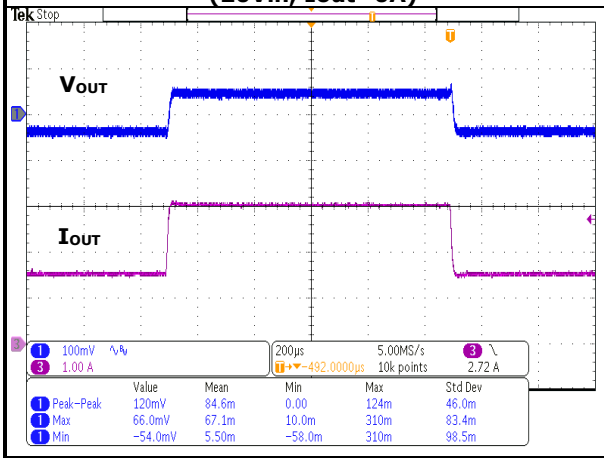


FIG.13 Transient Response (20Vin, 50% to 100% Load Step)

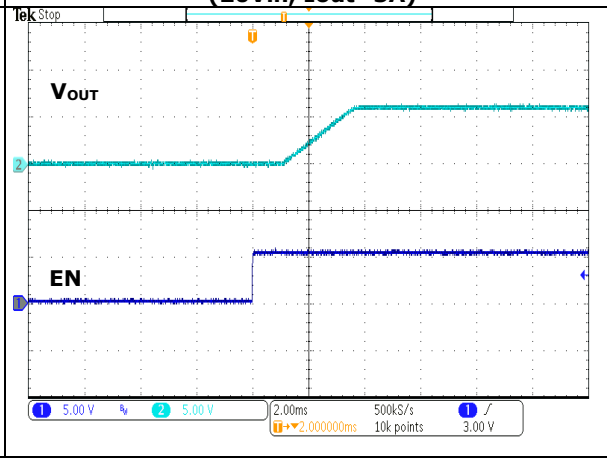


FIG.14 Turn-on (20Vin, Iout=0A)

TYPICAL PERFORMANCE CHARACTERISTICS: (7.0 VOUT)

Conditions: TA = 25 ºC, unless otherwise specified. Test Board Information: 30mm×30mm×1.6mm, 2 layers 2Oz. The output ripple and transient response measurement is short loop probing and 20MegHz bandwidth limited. Cin = 22uF/25V/1210X 2, Cout = 22uF/25V/1210X2 +56uF/25V (ESR:50mΩ)

The following figures provide the typical characteristic curves at 7.0Vout.

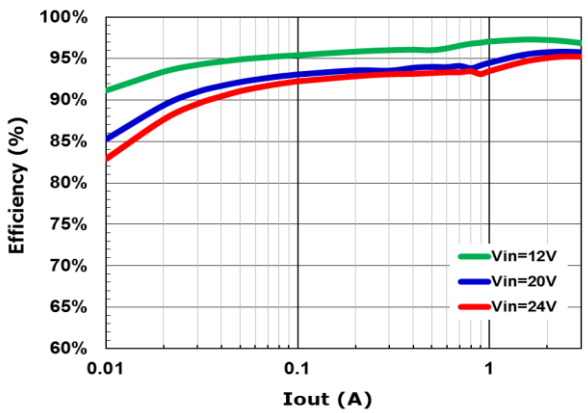


FIG.15 Efficiency V.S. Load Current

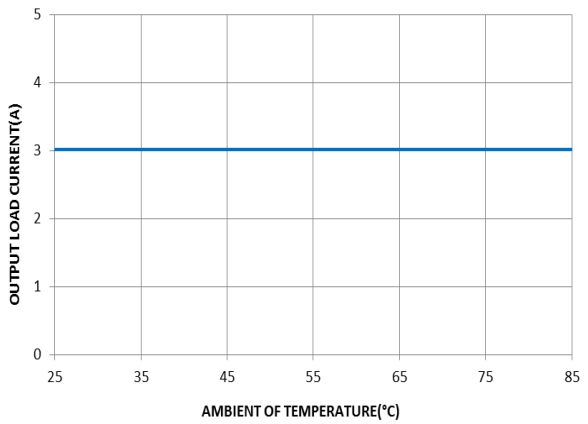


FIG.16 De-rating Curve

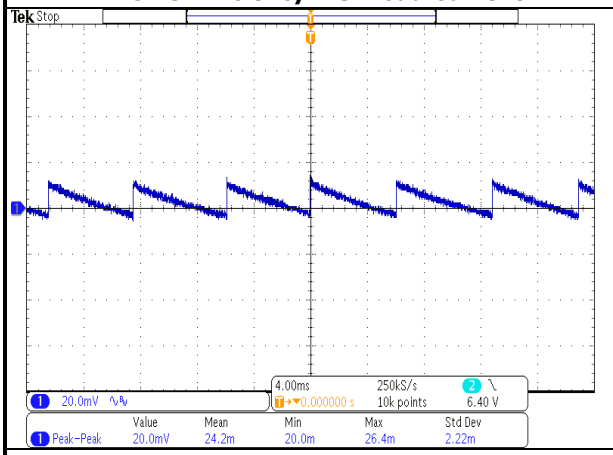


FIG.17 Output Ripple (20Vin, Iout=0A)

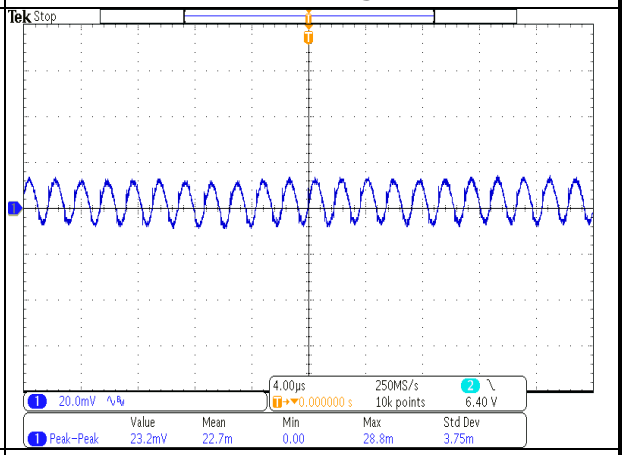


FIG.18 Output Ripple (20Vin, Iout=3A)

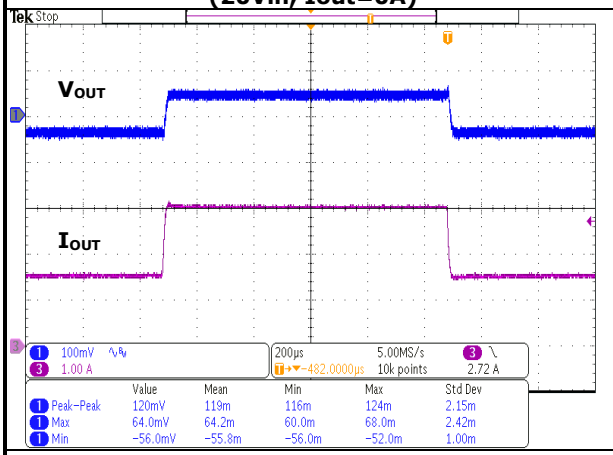


FIG.19 Transient Response (20Vin, 50% to 100% Load Step)

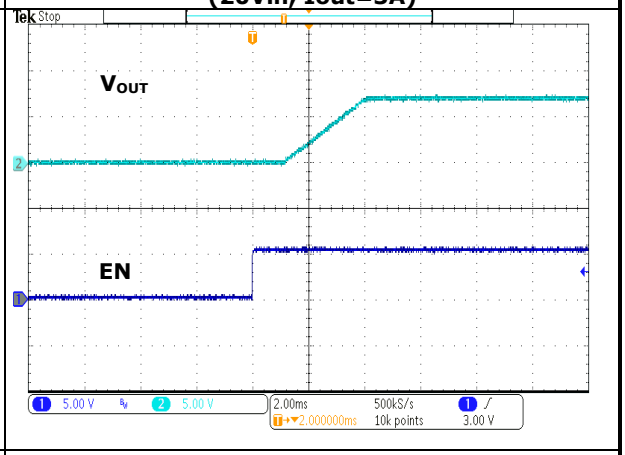


FIG.20 Turn-on (20Vin, Iout=0A)

TYPICAL PERFORMANCE CHARACTERISTICS: (8.0 VOUT)

Conditions: TA = 25 ºC, unless otherwise specified. Test Board Information: 30mm×30mm×1.6mm, 2 layers 2Oz. The output ripple and transient response measurement is short loop probing and 20MegHz bandwidth limited. Cin = 22uF/25V/1210X 2, Cout = 22uF/25V/1210X2 +56uF/25V (ESR:50mΩ)

The following figures provide the typical characteristic curves at 8.0Vout.

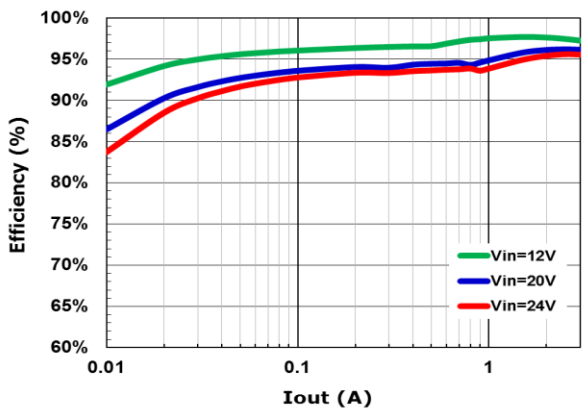


FIG.21 Efficiency V.S. Load Current

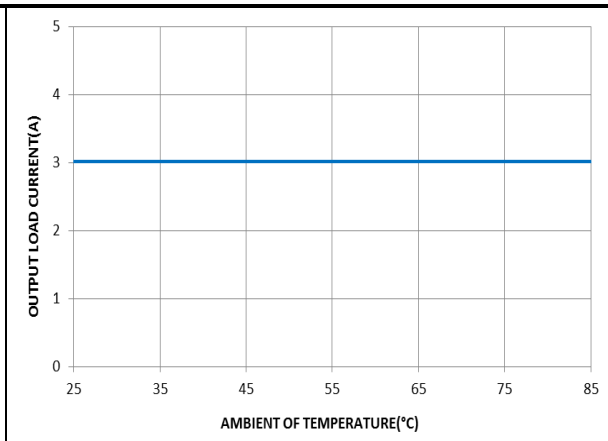


FIG.22 De-rating Curve

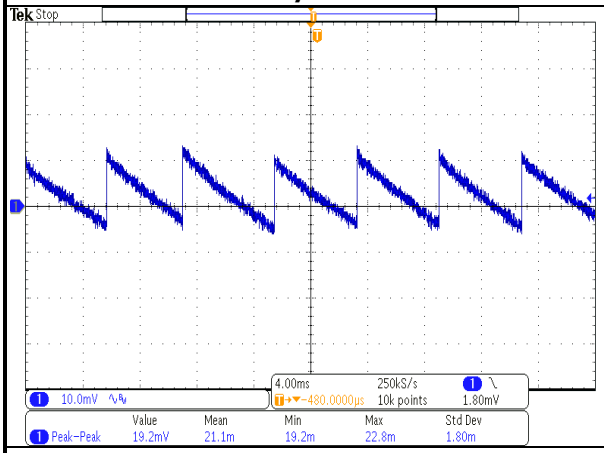


FIG.23 Output Ripple (20Vin, Iout=0A)

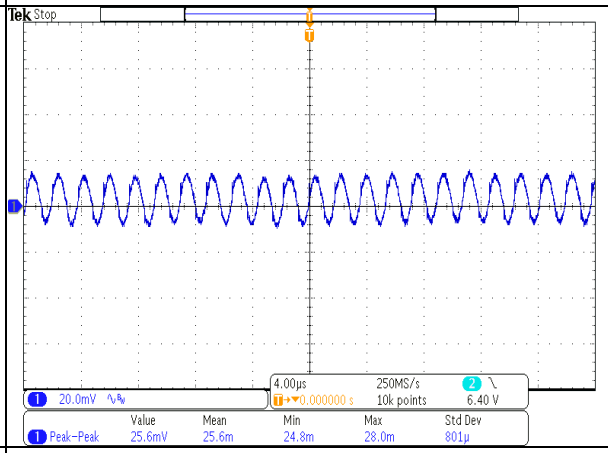


FIG.24 Output Ripple (20Vin, Iout=3A)

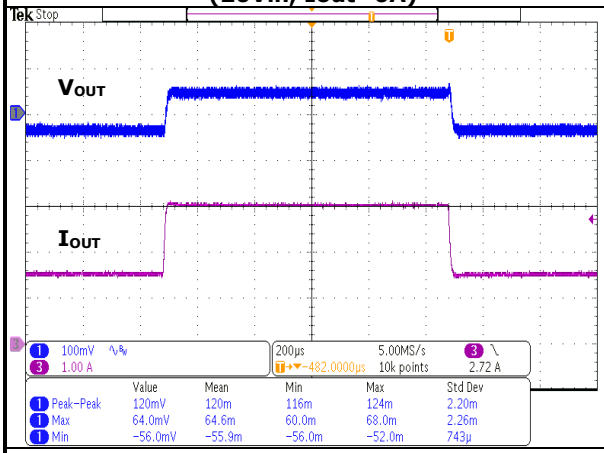


FIG.25 Transient Response (20Vin, 50% to 100% Load Step)

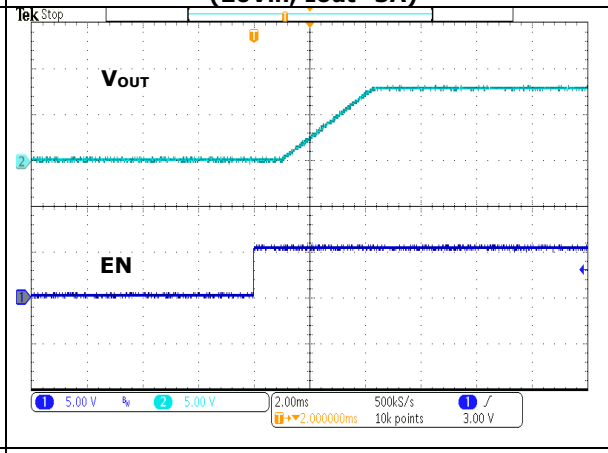


FIG.26 Turn-on (20Vin, Iout=0A)

TYPICAL PERFORMANCE CHARACTERISTICS: (9.0 VOUT)

Conditions: TA = 25 ºC, unless otherwise specified. Test Board Information: 30mm×30mm×1.6mm, 2 layers 2Oz. The output ripple and transient response measurement is short loop probing and 20MegHz bandwidth limited. Cin = 22uF/25V/1210X 2, Cout = 22uF/25V/1210X2 +56uF/25V (ESR:50mΩ)

The following figures provide the typical characteristic curves at 9.0Vout.

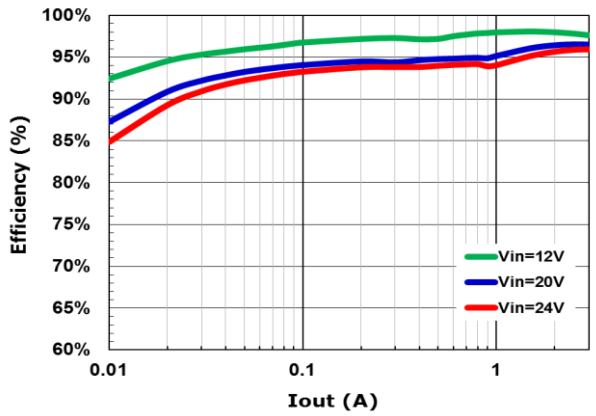


FIG.27 Efficiency V.S. Load Current

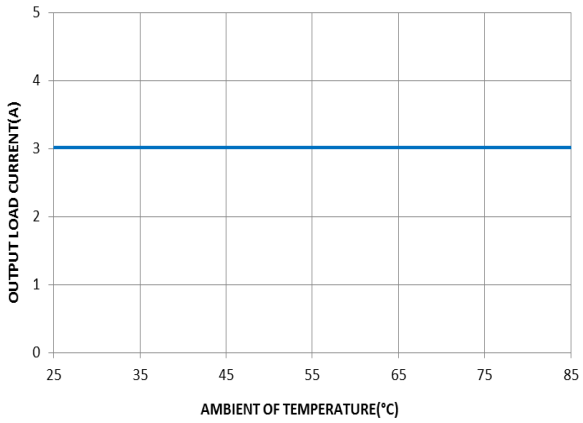


FIG.28 De-rating Curve

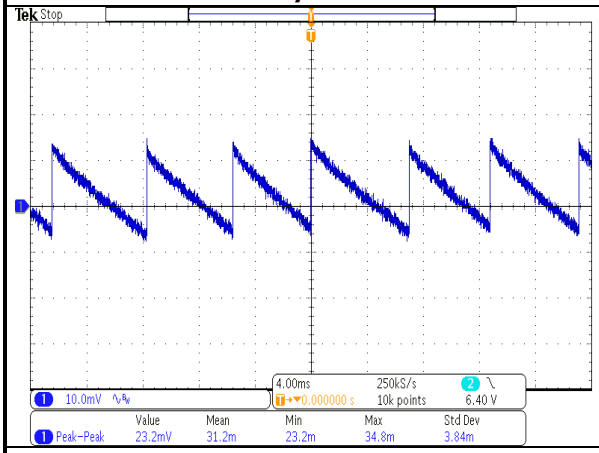


FIG.29 Output Ripple (20Vin, Iout=0A)

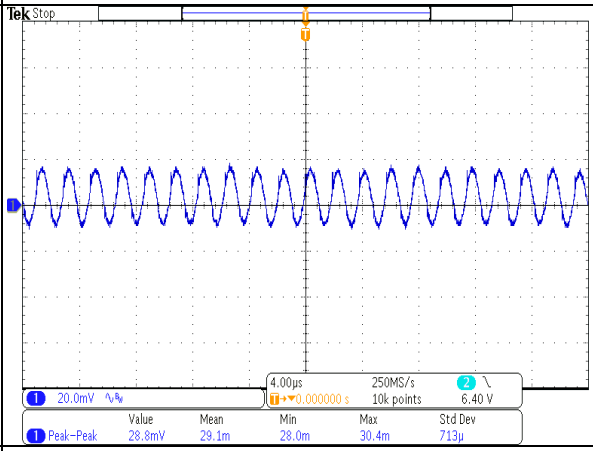


FIG.30 Output Ripple (20Vin, Iout=3A)

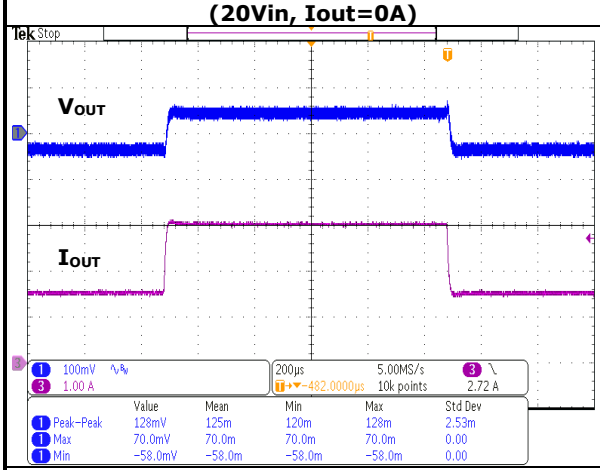


FIG.31 Transient Response (20Vin, 50% to 100% Load Step)

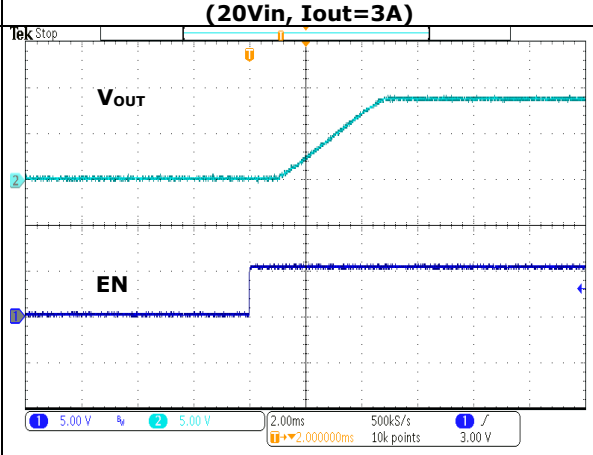


FIG.32 Turn-on (12Vin, Iout=0A)

TYPICAL PERFORMANCE CHARACTERISTICS: (12.0 VOUT)

Conditions: TA = 25 ºC, unless otherwise specified. Test Board Information: 30mm×30mm×1.6mm, 2 layers 2Oz.
The output ripple and transient response measurement is short loop probing and 20MegHz bandwidth limited.
Cin = 22uF/25V/1210X 2, Cout = 22uF/25V/1210X2 +56uF/25V (ESR:50mΩ)
The following figures provide the typical characteristic curves at 12.0Vout.

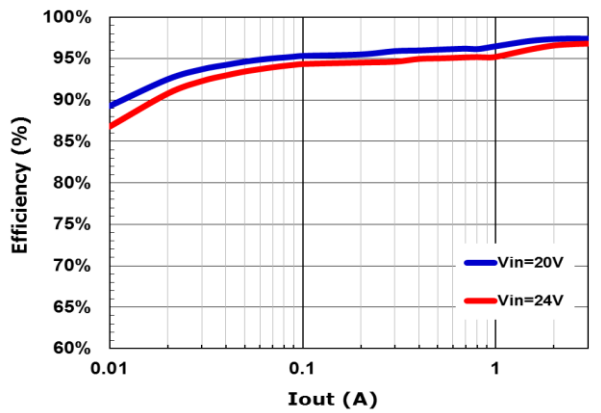


FIG.33 Efficiency V.S. Load Current

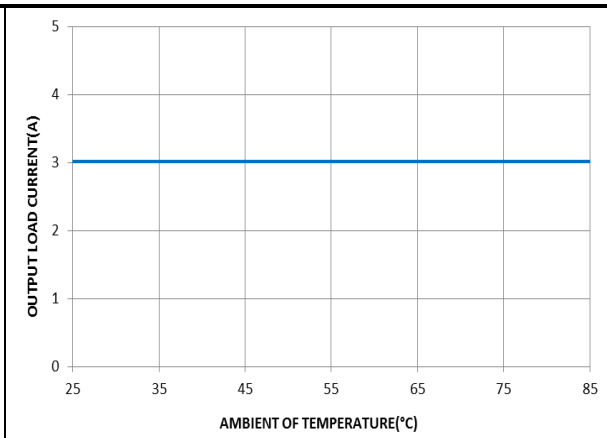


FIG.34 De-rating Curve

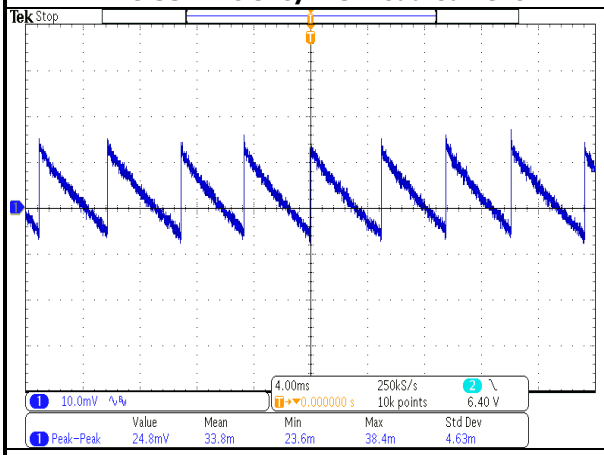


FIG.35 Output Ripple
(20Vin, Iout=0A)

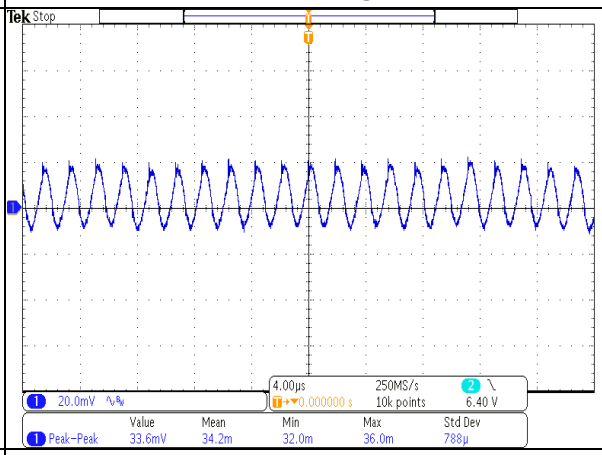


FIG.36 Output Ripple
(20Vin, Iout=3A)

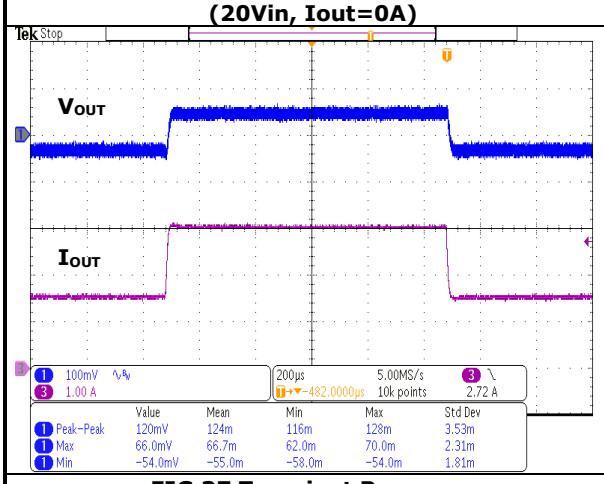


FIG.37 Transient Response
(20Vin, 50% to 100% Load Step)

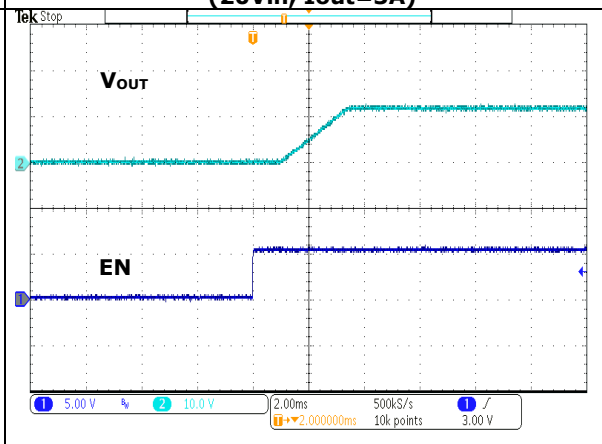


FIG.38 Turn-on
(20Vin, Iout=0A)

TYPICAL PERFORMANCE CHARACTERISTICS: (15.0 VOUT)

Conditions: TA = 25 ºC, unless otherwise specified. Test Board Information: 30mm×30mm×1.6mm, 2 layers 2Oz.
The output ripple and transient response measurement is short loop probing and 20MegHz bandwidth limited.
Cin = 22uF/25V/1210X 2, Cout = 22uF/25V/1210X2 +56uF/25V (ESR:50mΩ)
The following figures provide the typical characteristic curves at 15.0Vout.

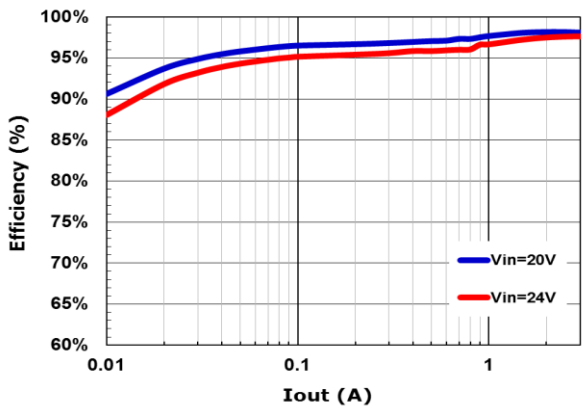


FIG.39 Efficiency V.S. Load Current

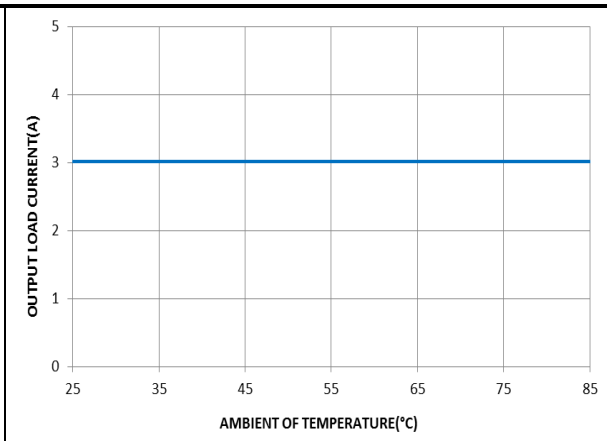


FIG.40 De-rating Curve

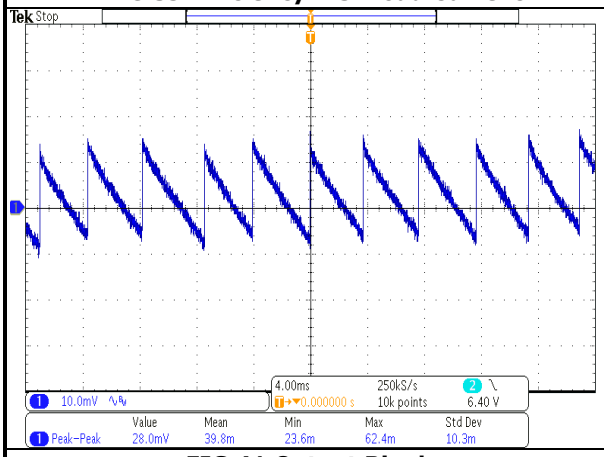


FIG.41 Output Ripple
(20Vin, Iout=0A)

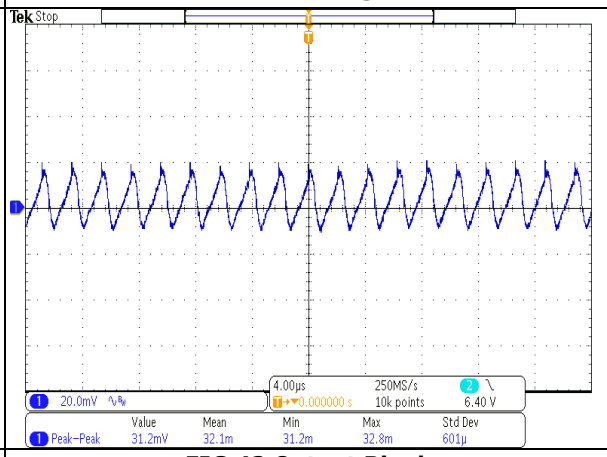


FIG.42 Output Ripple
(20Vin, Iout=3A)

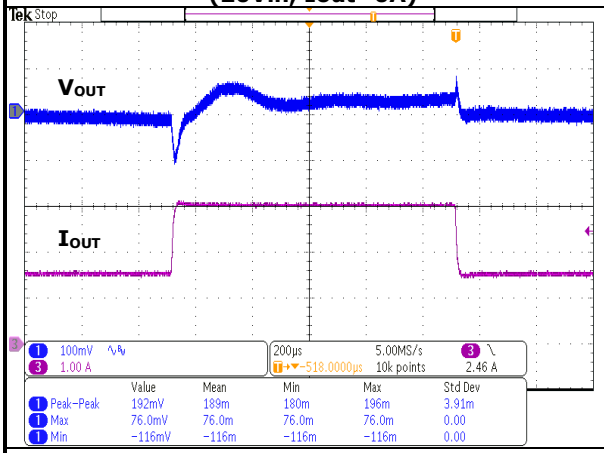


FIG.43 Transient Response
(20Vin, 50% to 100% Load Step)

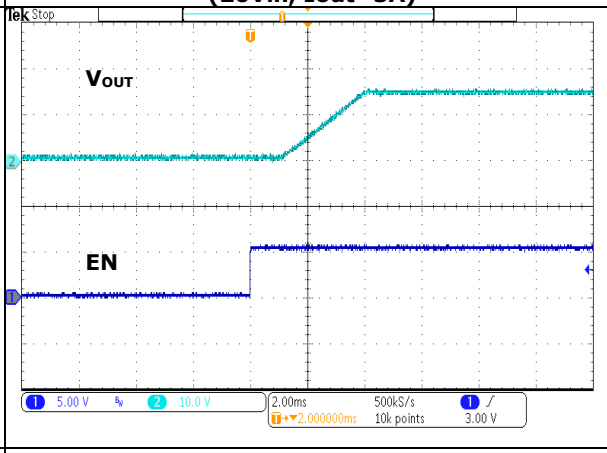


FIG.44 Turn-on
(20Vin, Iout=0A)

APPLICATIONS INFORMATION:

Detailed Description

MSN24VD03-GR is a 3A, synchronous buck converter with a fixed 5.1V LDO. It includes output line-drop compensation function to support accurate supply at the end of the cable for a varied load range. A programmable output voltage supports the USB PD requirement. A Quasi-PWM control is adapted in MSN24VD03-GR. It is a constant-on-time PWM control with input feed-forward while maintaining a relatively constant switching frequency. It advantages in the fast load-transient response compared with conventional constant-on-time PWM control. An EN pin is provided to turn on/off MSN24VD03-GR.

Constant-on-time PMW Control with Input Feed-Forward

The Quasi-PWM control algorithm can be described briefly: the high-side switch on-time is determined by a one-shot whose period is inversely proportional to input voltage and directly proportional to output voltage. Another on-shot determines the minimum off-time. The on-time one-shot can be triggered if the error comparator is low, the low side switch current is below the current-limit threshold, and the minimum off-time one-shot has timed out.

UVLO and Soft-Start

When VCC is below 4V, under-voltage lockout (UVLO) inhibits switching and forces DL to high. It reset the fault latch and soft-start counter. An internal soft-start timer ramps up the current limit threshold to 100% of current limit setting within 2.5ms.

Accurate Output Over Current Limit

MSN24VD03-GR provides the lower output over current protection by external sense resistor, R sense. Please refer to below equation to get the lower limit.

$$I_{OCP} = 66mV / (15m + R_{SENSE})$$

Output Line-drop Compensation

Connecting the I_{CS} pin to a R_{SENSE} divider and adjust the output voltage drop due to cable resistance loss between the regulator and the load.

$$V_{DROP} = V_{WIRE} = 3 \times I_{OUT} \times (15m + R_{SENSE})$$

APPLICATIONS INFORMATION:

Programmable Output Voltage

Output voltage is programmed by VID0, VID1 and VID2 as show in Table 1.It supports dynamic voltage scaling (DVS) to change VOUT during SMPS operation. If output voltage set to 20V, please keep input voltage between 20V to 21V.

.

VID2	VID1	VID0	Output Voltage
0	0	0	5.1V
0	0	1	6V
0	1	0	7V
0	1	1	8V
1	0	0	9V
1	0	1	12V
1	1	0	15V
1	1	1	20V

Table 1: Output Voltage Setting

RECOMMENDATION LAYOUT GUIDE:

In order to achieve stable, low losses, less noise or spike, and good thermal performance several layout considerations are necessary. The recommendation layout is shown as Figure 45.

1. If the application of module is fixed output, 0 means VIDX connected to SGND (Pin F5), do not connected to GND directly.
2. Connect GND and SGND together close to the negative terminal of COUT with single trace.

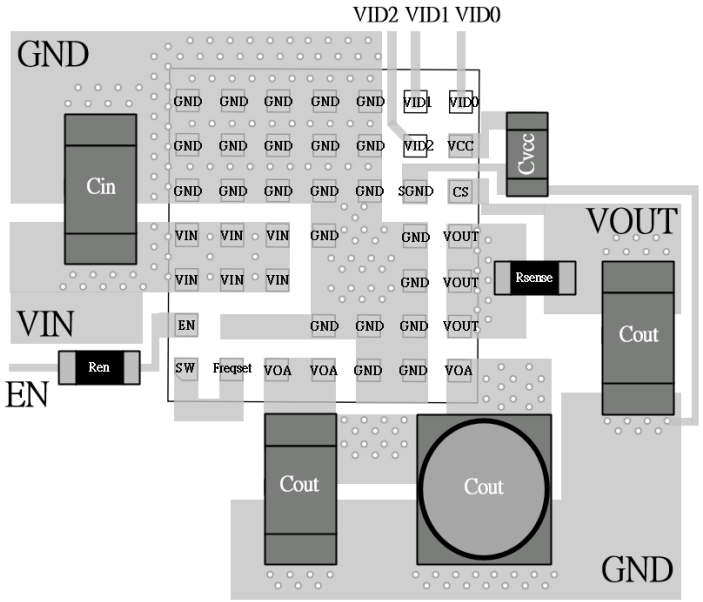


FIG.45 Recommendation Layout

REFLOW PARAMETERS:

Lead-free soldering process is a standard of electronic products production. Solder alloys like Sn/Ag, Sn/Ag/Cu and Sn/Ag/Bi are used extensively to replace the traditional Sn/Pb alloy. Sn/Ag/Cu alloy (SAC) is recommended for this power module process. In the SAC alloy series, SAC305 is a very popular solder alloy containing 3% Ag and 0.5% Cu and easy to obtain. Figure 46 shows an example of the reflow profile diagram. Typically, the profile has three stages. During the initial stage from room temperature to 150°C, the ramp rate of temperature should not be more than 3°C/sec. The soak zone then occurs from 150°C to 200°C and should last for 60 to 120 seconds. Finally, keep at over 217°C for 60 seconds limit to melt the solder and make the peak temperature at the range from 240°C to 250°C. It is noted that the time of peak temperature should depend on the mass of the PCB board. The reflow profile is usually supported by the solder vendor and one should adopt it for optimization according to various solder type and various manufacturers' formulae.

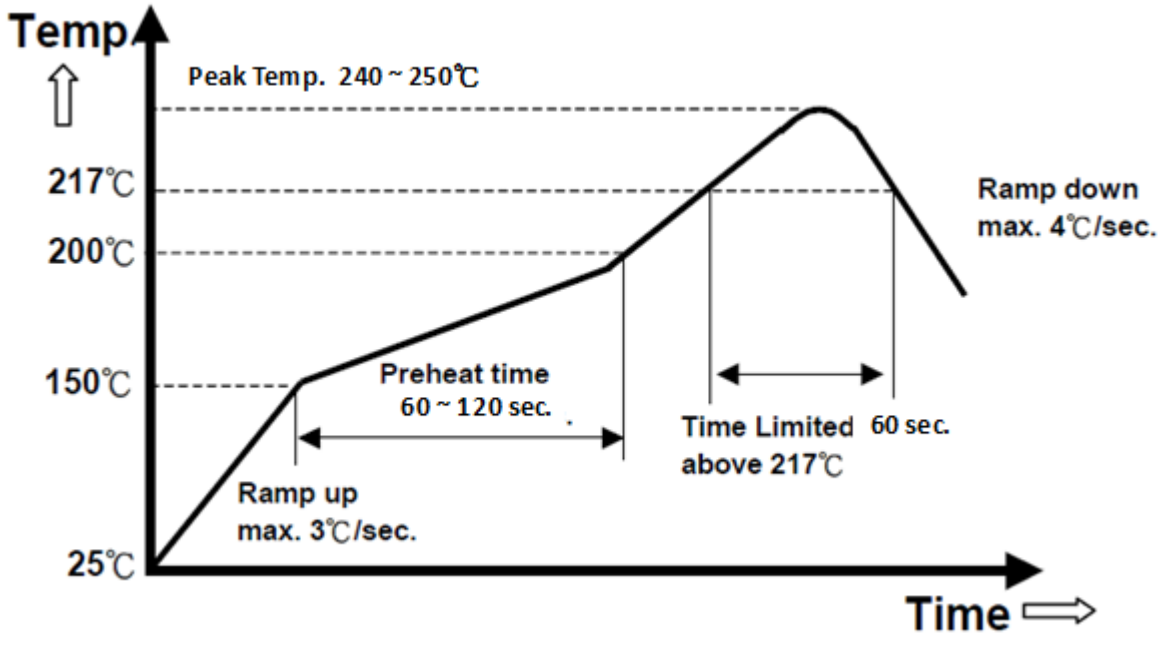
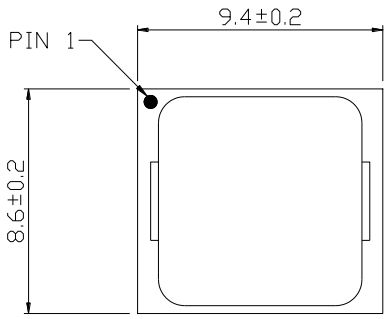


FIG.46 Recommendation Reflow Profile

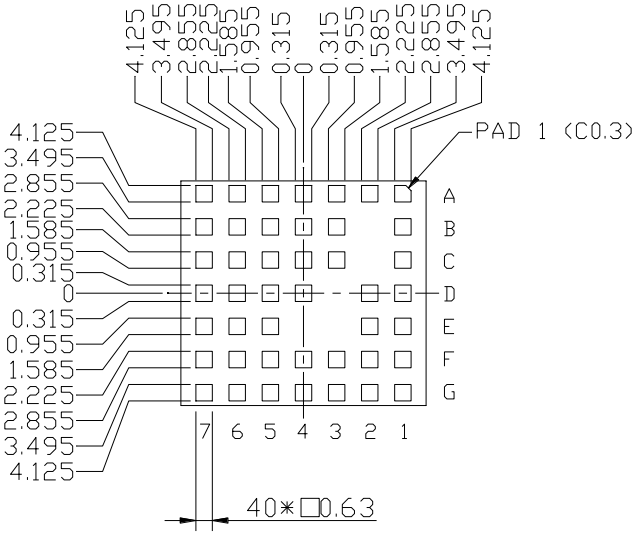
PACKAGE OUTLINE DRAWING:

Unit: mm

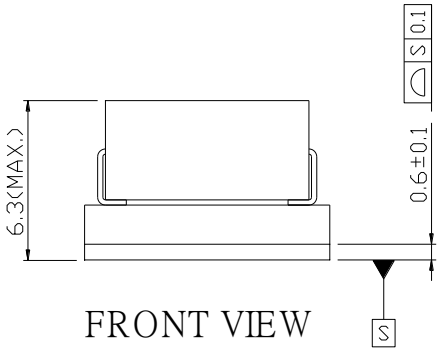
General Tolerances:±0.2mm



TOP VIEW



BOTTOM VIEW



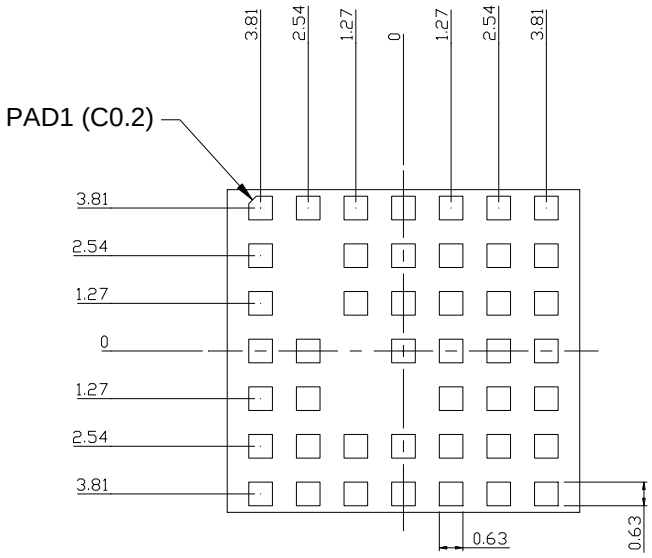
FRONT VIEW

*All dimensions in mm
*Tolerance: X.X±0.2
X.XX±0.15
X.XXX±0.10

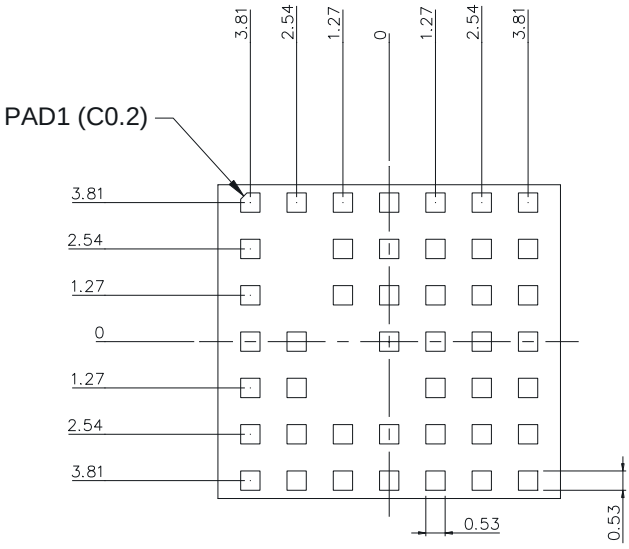
PACKAGE OUTLINE DRAWING:

Unit: mm

General Tolerances:±0.2mm



TOP VIEW
TYPICAL RECOMMENDED LAND PATTERN

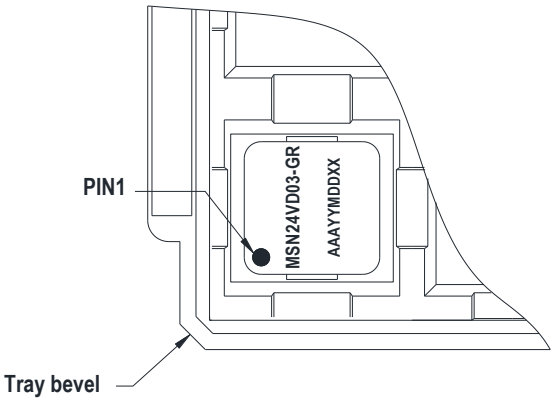


TOP VIEW
STENCIL PATTERN WITH PADS

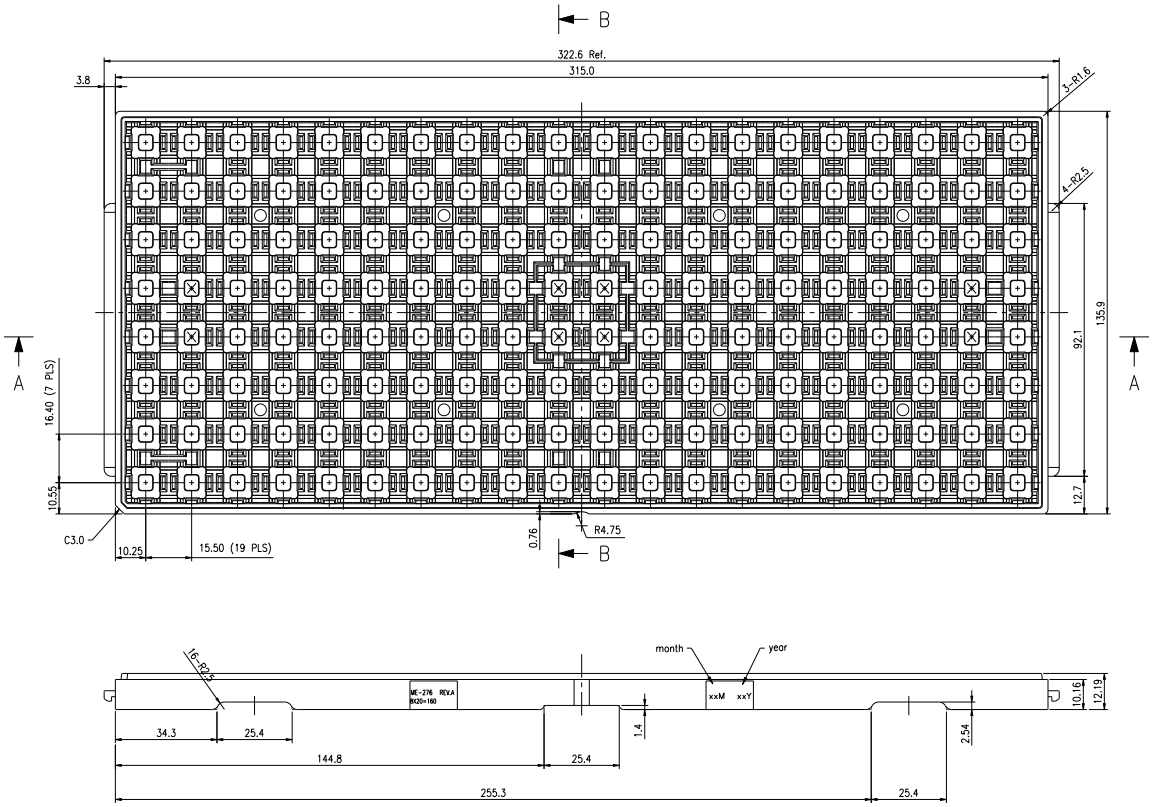
PACKING INFORMATION:

Unit: mm

Tray Packing



PACKAGE IN TRAY LOADING ORIENTATION



TRAY DIMENSION

REVISION HISTORY:

Date	Revision	Changes
	00	Release the preliminary specification.
2018.03.07	01	Add packing and marking drawing.
2019.04.22	02	Update packing information, change Tape/Real to Tray
2019.07.09	03	1.Update Rth(jchoke-a) to Rth(jc) 2.Update STENCIL PATTERN WITH SQUARE PADS to STENCIL PATTERN WITH PADS
2020.07.13	04	1.Update page 4 Rth(ja)