High Efficiency POL Datasheet

Digital DC/DC Power Module with SMBus/PMBus MSN12AD60-RUD

FEATURES:

- Maximum Load:60A
- Input Voltage Range from 8V to 15V
- Output Voltage Range from 0.6V to 1.8V
- Configurable Digital Loop Compensation
  - Auto-Control Real-Time Adaptive Loop Compensation
- SMBus Interface with PMBus Power System Management Protocol
- Precision Measurement & Telemetry Reporting: VOUT, IOUT, VIN, EOUT, Temperature, Fsw, Duty Cycle
- Programmable Protection & Warning
  - Output OVP, OCP,SCP, UV, LOS Warning
  - Input UVLO, OVLO
  - Internal & External OTP
  - Phase Loss fault
  - Temperature Compensated Faults
  - Configurable SALRT
- Single-Pin Configuration with Eight Profile Tables
- Power Management and Conversion
  - SwitchFrequencyto500kHz
  - Programmable VOUT, Voltage Tracking, Margining, & Sequencing
  - Adjustable Load-Line
  - Power Good, System Good, & Remote Power Down
- 16mmX16mmX7.5mm (Typical) BGA Package

APPLICATIONS:

- VDDQ for DDR Memory; Supports Over-Clocking Applications
- ASIC, FPGA, Microprocessor, Memory
- Networking, Communications, Storage, Server, Computing
- Advanced Power Modules & General Purpose POL

GENERAL DESCRIPTION:

The MSN12AD60-RUD is a digital synchronous DC/DC power module. The digital controller, power MOSFETs and most of support components are integrated in one hybrid package.

The module allows system telemetry (remote measurement and reporting) of current, voltage, and temperature information through its serial interface. Additionally, to maximize system performance and reliability, the module provides temperature correction/compensation of several parameters. The module is a fully protected DC/DC solution that utilizes analog and digital functionality to maximize protection of the system.

The compact size enables utilization of space for highly density point of load to save the space and area. The thermal pad can enhance heat transferring capability. It is suitable for automated assembly by standard surface mount equipment and is Pb-free and RoHS-compliance.

TYPICAL APPLICATION CIRCUIT

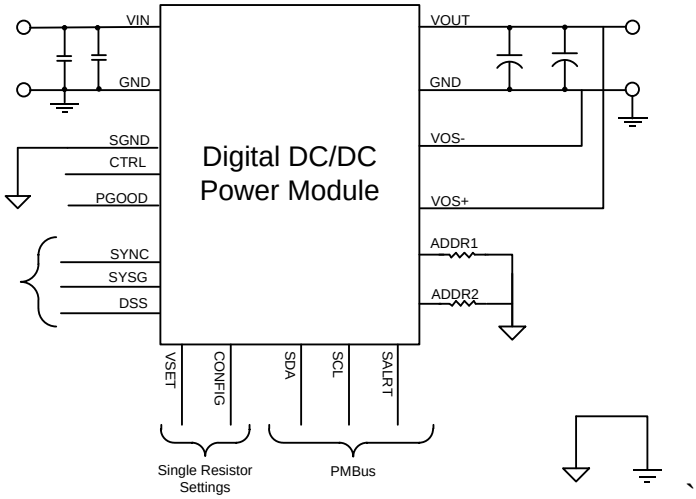


FIGURE.1TYPICAL APPLICATION FOR POWER MODULE OPERATION

TYPICAL APPLICATION CIRCUIT

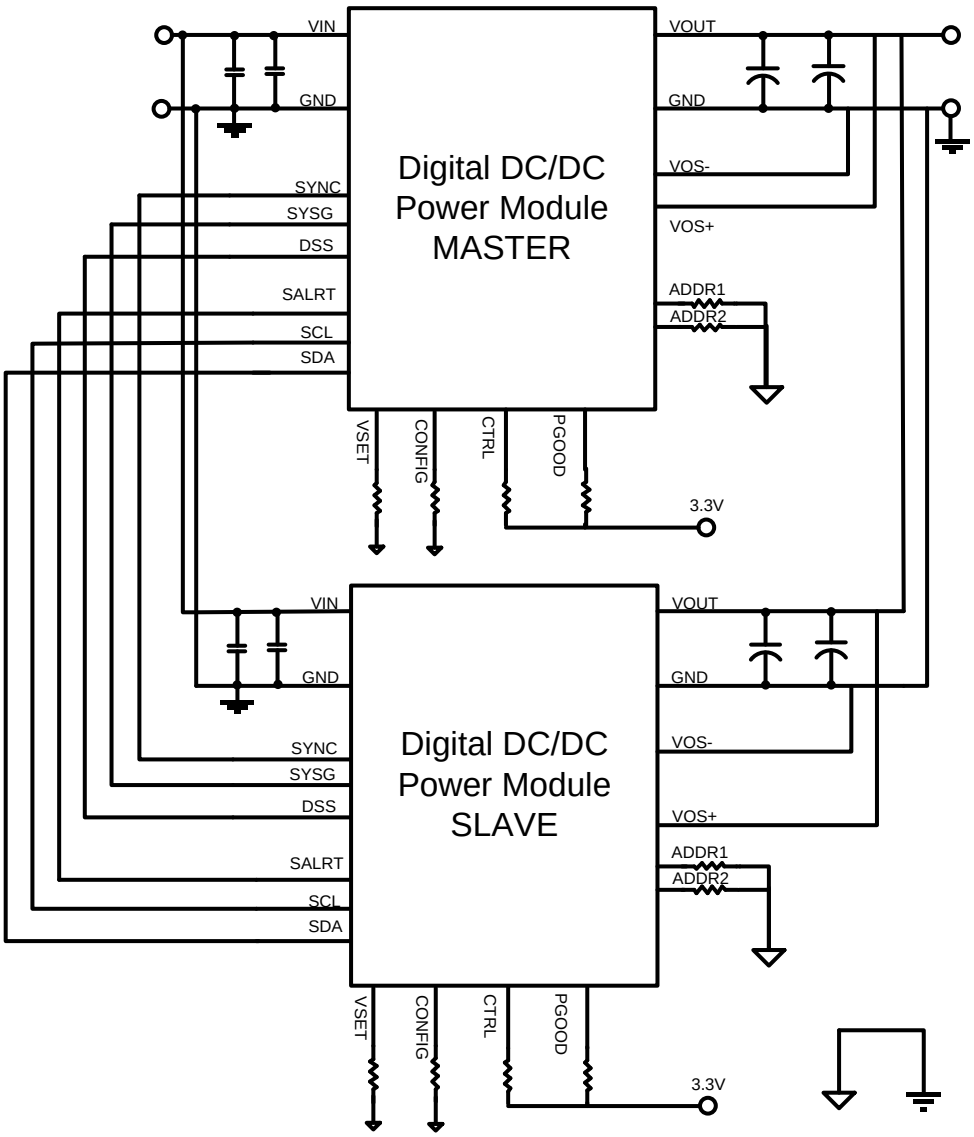


FIGURE.2TYPICAL APPLICATION FOR POWER MODULE PARALLELED OPERATION

Recommend Capacitor:

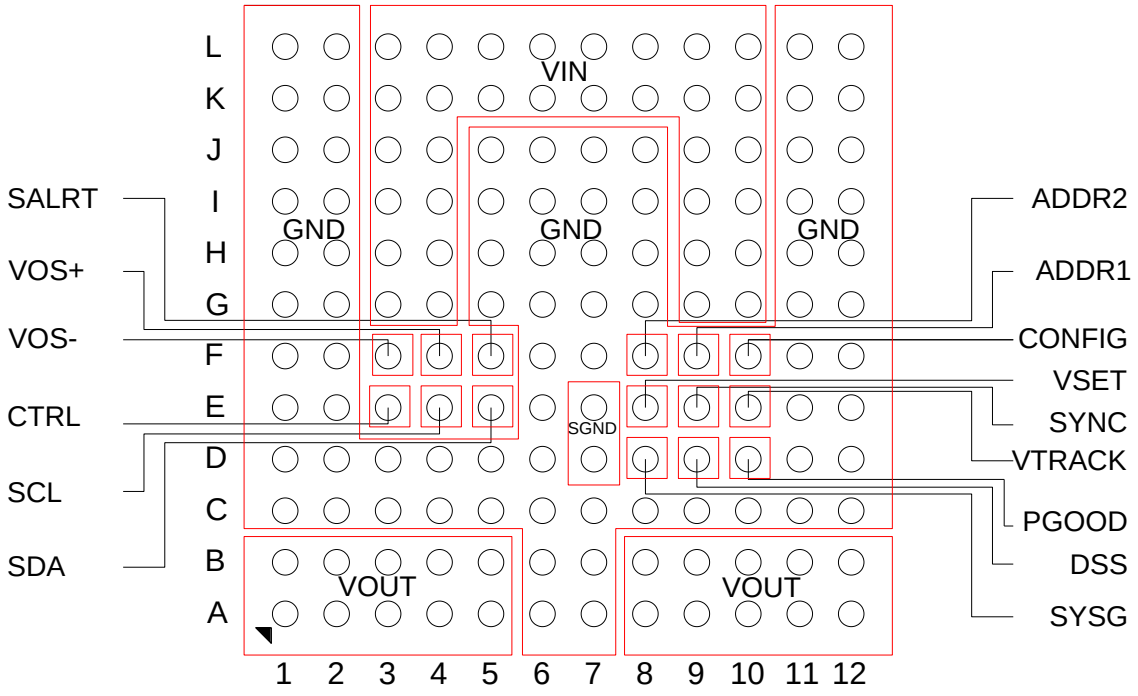
- **Input: MLCC 22uF/25V/1210x8, 4.7uF/25V/0805×4 for Two Phase**
- **Output: MLCC100uF/6.3V/1210×12,POSCAP 470uF/2.5V x8 for Two Phase**

ORDER INFORMATION:

Part Number	Ambient Temp. Range (°C)	Package (Pb-Free)	MSL	Note
MSN12AD60-RUD	-40 ~ +85	BGA	Level 3	-

Order Code	Packing	Quantity
MSN12AD60-RUD	Tray	65

PIN CONFIGURATION:



TOP VIEW

PIN DESCRIPTION:

Symbol	#	Type	Description
VIN	L3-L10,K3-K10,J3-J4 J9-J10,I3-I4,I9-I10, H3-H4,H9-H10,G3-G4, G9-G10	PWR	Power input pin. It needs to connect input rail and using for heat transferring to heat dissipation layer by Vias connection. Place the input ceramic type capacitor as closely as possible to this pin.
GND	L1-L2,L11-L12,K1-K2, K11-K12,J1-J2,J5-J8, J11-J12,I1-I2,I5-I8, I11-I12,H1-H2,H5-H8, H11-H12,G1-G2,G5-G8, G11-G12,F1-F2,F6-F7, F11-F12,E1-E2,E6,E11-E12, D1-D6,D11-D12,C1-C12, B6-B7,A6-A7	PWR	Power ground pin. It needs to connect one or more ground plane directly and using for heat transferring to heat dissipation layer by Vias connection. Place the input ceramic type and output capacitors as closely as possible to this pin.
VOUT	B1-B5,B8-B12,A1-A5, A8-A12	PWR	Power output pin. Connect to output and using for heat transferring to heat dissipation layer by Vias connection. Place the output capacitors as closely as possible to this pin.
VOS+	F4	Analog I	Differential output voltage sense (positive).
VOS-	F3	Analog I	Differential output voltage sense (negative).
SALRT	F5	Digital O	PMBus alert line. When low, signals to the host that a fault condition exists.
ADDR2	F8	Analog IO	A resistor from ADDR2 to SGND can be used to set the PMBus address.
ADDR1	F9	Analog IO	A resistor from ADDR1 to SGND can be used to set the PMBus address.
CONFIG	F10	Analog I Digital O	A resistor from CONFIG to SGND can be used to select a configuration table.
CTRL	E3	Digital I	PMBus-compatible control pin with programmable functionality. CTRL should never be left floating.

PIN DESCRIPTION:(Cont.)

Symbol	#	Type	Description
SCL	E4	Digital I	PMBus serial clock input.
SDA	E5	SDA	PMBus serial data IO.
SGND	E7,D7	GND	Signal ground pin for overall signal reference used.
VSET	E8	Analog I	A resistor from VSET to GND can be used to program the VOUT set-point.
SYNC	E9	Digital IO	Used for frequency synchronization and phase alignment between MSN12AD60-RUDs. SYNC is an input if module is configured as a SYNC slave. Otherwise SYNC is a push-pull output. SYNC has a weak internal pull-up.
VTRACK	E10	Analog I	Voltage reference input if module is configured for voltage tracking mode.
SYSG	D8	Digital IO	Open-drain fault input/output. May be wired-AND connection with other MSN12AD60-RUDs. A de-asserted SYSG will inhibit power conversion. SYSG has a weak internal pull-up.
DSS	D9	Digital IO	Digital Stress Share. Digital stress share signal between multiple module MSN12AD60-RUDs. DSS has a weak internal pull-up.
PGOOD	D10	Digital O	Open-drain Power Good output. May be used for wired-SND connection between MSN12AD60-RUDs. Asserted if output slope has reached new set-point and no fault exists. PG has a weak internal pull-up.

ELECTRICAL SPECIFICATIONS:

CAUTION: Do not operate at or near absolute maximum rating listed for extended periods of time. This stress may adversely impact product reliability and result in failures not covered by warranty.

Parameter	Description	Min.	Typ.	Max.	Unit
■ Absolute Maximum Ratings					
VIN to GND	Note 1	-	-	+16.0	V
VOUT to GND	Note 1	-	-	+2.0	V
CTRL to GND	Note 1	-	-	+3.6	V
PGOOD to GND	Note 1			+3.6	V
VOS+ to GND	Note 1			+3.6	V
VOS- to GND	Note 1			+0.3	V
VTRACK to GND	Note 1			+3.6	V
Tc	Case Temperature of Inductor	-	-	+110	℃
Tstg	Storage Temperature	-40	-	+125	℃
■ Recommendation Operating Ratings					
VIN	Input Supply Voltage	+8.0	-	+15.0	V
VOUT	Adjusted Output Voltage	+0.6		+1.8	V
Ta	Ambient Temperature	-40	-	+85	℃
■ Thermal Information					
Rth(j_{choke}-a)	Thermal resistance from junction to ambient (Note 2)	-	9.2	-	°C/W

NOTES:
1 Parameters guaranteed by power IC vendor design and test prior to module assembly.
2 Rth(j_{choke}-a)is measured with the component mounted on an effective thermal conductivity test board on 0 LFM condition. The test board size is 110mm×100mm×1.6mm with 4 layers. The test condition is complied with JEDEC EIJ/JESD 51 Standards and VIN=12V VOUT=0.85.

ELECTRICAL SPECIFICATIONS:(Cont.)

Conditions: T_A = 25 ºC,unless otherwise specified.
VIN=12V, VOUT=1.0V,Cin= 22uF/16V/1210×6, 4.7uF/25V/0805×2, Cout = 100uF/6.3V/1210×6, POSCAP 470uF/2.5V×4.
Test Board Information: 110mm×100mm×1.6mm, 4 layers.

Symbol	Parameter	Conditions	Min.	Typ.	Max.	Unit
■ Input Characteristics						
$I_{Q(IN)}$	Input supply bias current	Vin= 12V, Iout=0A Vout =1.0V, CTRL =3.3V	-	0.2	-	mA
$I_{S(IN)}$	Input supply current	Vin= 12V, CTRL = 3.3V				
		Iout = 5mA,Vout =1.0V	-	100	-	mA
		Iout = 60A,Vout =1.0V, Frequency=500kHz	-	5.7	-	A
■ DC Parameters						
VIH	Input High Voltage	DSS, SYSG, SYNC.	2.0			V
VIL	Input Low Voltage	DSS, SYSG, SYNC.			0.8	V
■ Output Characteristics						
I_{OUT}(DC)	Output continuous current range		0	-	60	A
V_{OUT}(DC)	Output Voltage Accuracy	Vin=12V Vout=1.0V	-0.5		+0.5	% $V_{O(SET)}$
ΔVOUT /ΔVOUT	Line regulation accuracy	Vin= 7.0V to 15V Vout= 1.0V, Iout=0A Vout = 1.0V, Iout =60A	-	1		% $V_{O(SET)}$
ΔVOUT /VOUT	Load regulation accuracy	Iout = 0A to 30A Vin = 12V, Vout = 1.0V	-	1	-	$\%_{(SET)}$
V_{OUT}(AC)	Output ripple voltage	Vin = 12V, Vout = 1.0V CTRL=High 20MHz BW	-	-	-	-
		IOUT = 30A		15		mVp-p
■ Dynamic Characteristics						
ΔV_{OUT-DP}	Voltage change for positive load step	Iout = 0 A to 15A Current slew rate = 2.5A/uS Vin = 12V, Vout = 1.0V	-	30	-	mVp-p
ΔV_{OUT-DN}	Voltage change for negative load step	Iout =15A to 0A Current slew rate = 2.5A/uS Vin = 12V, Vout = 1.0V	-	30	-	mVp-p
■ Oscillator And Switching Characteristics						
F_{OSC}	Oscillator frequency	Factory setting	-	500	-	kHz
V_{CTRL_TH}	Enable rising threshold voltage		1.5	-	-	V
	Enable falling threshold voltage		-	-	0.8	V
V_{POOD}	Power Good Threshold				90	%
	Power Good Delay		-	-	1.1	ms
Efficiency		VIN=12V VOUT=1.0V IOUT=60A	-	87		%
Output Voltage Startup Delay			-	8	10	ms

ELECTRICAL SPECIFICATIONS:(Cont.)

Conditions: T_A = 25 ºC,unless otherwise specified.
VIN=12V, VOUT=1.0V,Cin= 22uF/16V/1210×6, 4.7uF/25V/0805×2, Cout = 100uF/6.3V/1210×6, POSCAP 470uF/2.5V×4.
Test Board Information: 110mm×100mm×1.6mm, 4 layers.

Symbol	Parameter	Conditions	Min.	Typ.	Max.	Unit
■ Serial Communication PMBUS DC Characteristics						
VIH	Input High Voltage	SCL, SDA	2.1		3.3	V
VIL	Input Low Voltage	SCL, SDA			0.8	V
IOL	Input Leakage Current	SCL, SDA, SALRT, CTRL.	-10		10	uA
VOL	Output Low Voltage	SDA, SALRT. At rated pull-up current.			0.4	V
CPIN	Pin Capacitance	SCL, SDA, SALRT.			10	pF
■ Serial Communication PMBUS Timing Characteristics						
f_{SMB}	Operating Frequency		10		400	kHz
t_{BUF}	Between Stop and Start condition		1.3			us
$t_{HD:STA}$	Hold Time	After this period the first clock is generated.	0.6			us
$t_{SU:STA}$	Repeated StartConditionSetup Time		0.6			us
$t_{SU:STO}$	Stop Condition Setup Time		0.6			us
$t_{HD:DAT}$	Data Hold Time	Transmitting data.	300			ns
		Receiving data.	0			ns
$t_{SU:DAT}$	Data Setup Time		100			ns
t_{LOW}	Clock Low Period		1.3			us
t_{HIGH}	Clock High Period		0.6		50	us
t_F	Clock/Data Fall Time		20		300	ns
t_R	Clock/Data Rise Time		20			ns
■ Fault Protection Characteristics						
UVLO	UVLO threshold Range	Configurable via I2C/SMBus	7.5			V
OUV	Output under voltage threshold	Factory setting		0.510		V
OVP	Output over voltage threshold	Factory setting		15		%
OTP	Thermal protection threshold	Factory setting		150		℃
OCP	Over current protection	Factory setting		72		A
VPG	Power-Good VOUT Threshold	Factory setting		12		%Vout

TYPICAL PERFORMANCE CHARACTERISTICS: (VOUT=0.8V)

Conditions: T_A = 25 ºC,unless otherwise specified.
VIN=12V, VOUT=1.0V,Cin= 22uF/16V/1210×4, 4.7uF/25V/0805×2, Cout = 100uF/6.3V/1210×6, POSCAP 470uF/2.5V×4.
The output ripple and transient response measurement is short loop probing and 20MegHz bandwidth limited.
Test Board Information: 110mm×100mm×1.6mm, 4 layers.

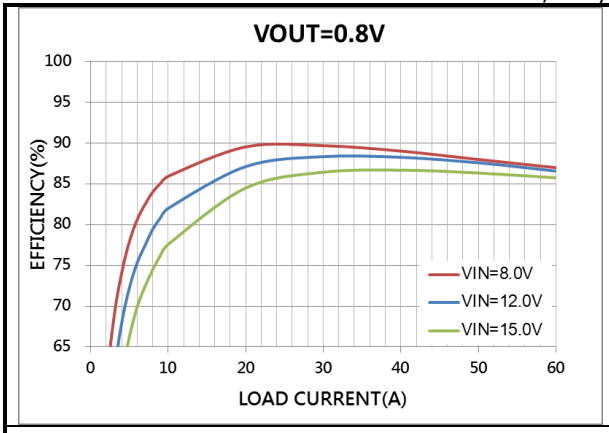


FIG.3EFFICIENCY V.S. LOAD CURRENT (VIN=12V, VOUT=0.8V)

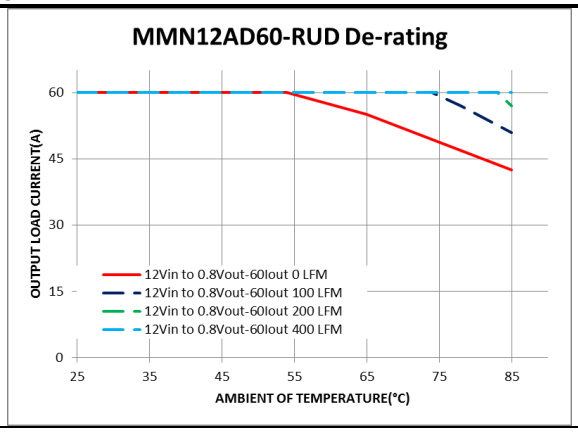


FIG.4DE-RATING CURVE (VIN=12V, VOUT=0.8V)

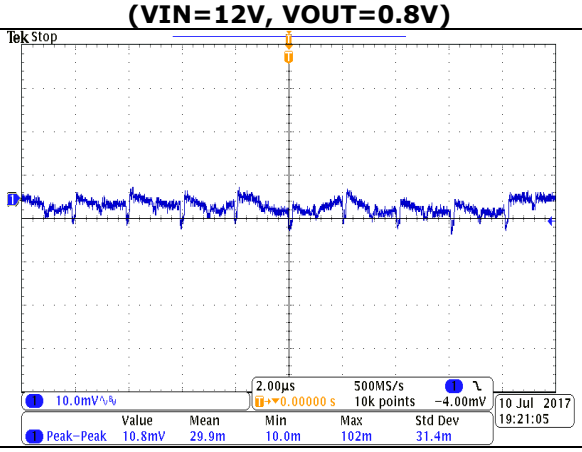


FIG.5 OUTPUT RIPPLE (12VIN, 0.8VOUT, IOUT=0A)

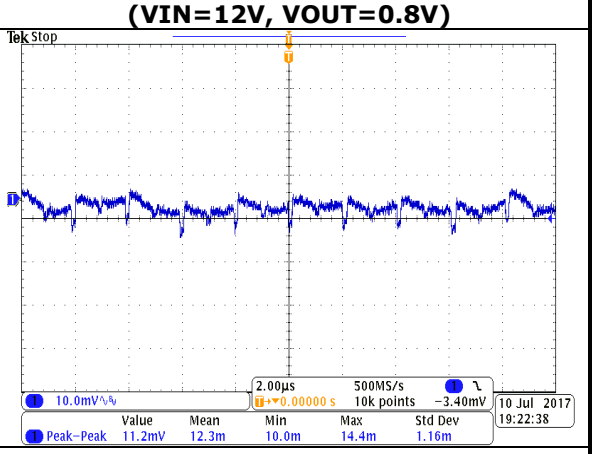


FIG.6 OUTPUT RIPPLE (12VIN, 0.8VOUT, IOUT=60A)

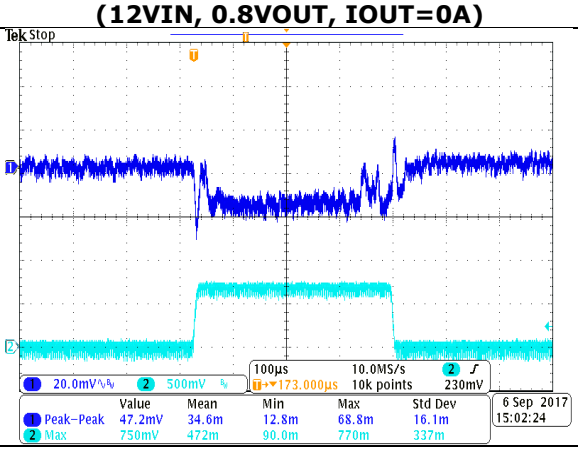


FIG.7 TRANSIENT RESPONSE (12VIN, 0.8VOUT, 0% to 50% LOAD STEP) With Resistor Load 24mΩ

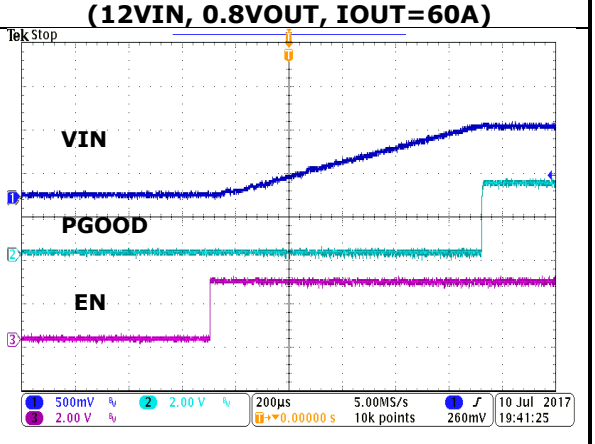


FIG.8 TURN-ON (12VIN, 0.8VOUT, IOUT=0A)

TYPICAL PERFORMANCE CHARACTERISTICS: (VOUT=0.85V)

Conditions: T_A = 25 ºC,unless otherwise specified.
VIN=12V, VOUT=1.0V,Cin= 22uF/16V/1210×4, 4.7uF/25V/0805×2, Cout = 100uF/6.3V/1210×6, POSCAP 470uF/2.5V×4.
The output ripple and transient response measurement is short loop probing and 20MegHz bandwidth limited.
Test Board Information: 110mm×100mm×1.6mm, 4 layers.

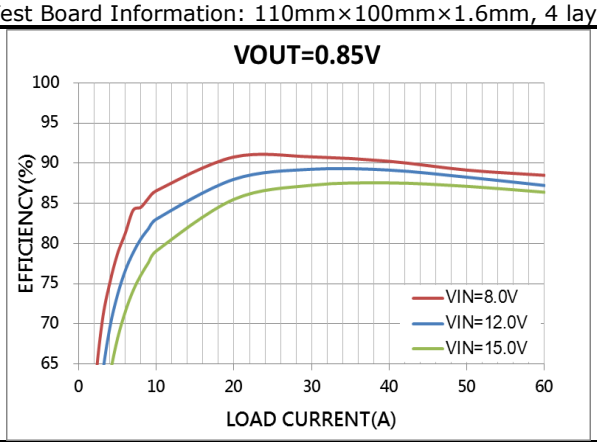


FIG.9EFFICIENCY V.S. LOAD CURRENT (VIN=12V, VOUT=0.85V)

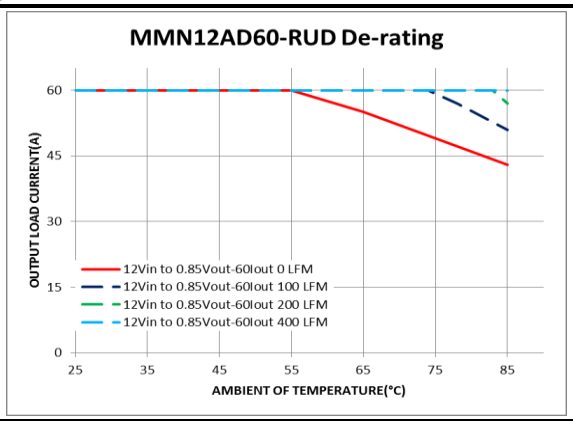


FIG.10DE-RATING CURVE (VIN=12V, VOUT=0.85V)

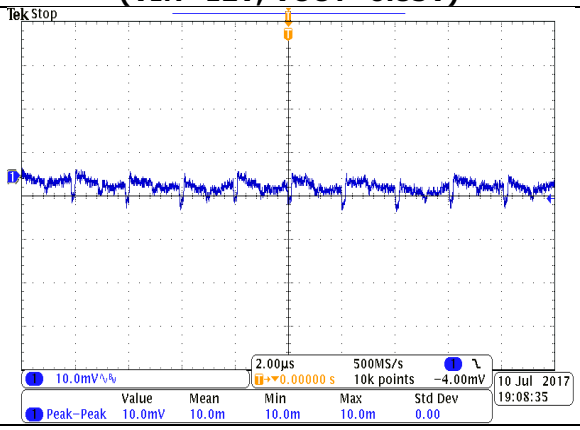


FIG.11 OUTPUT RIPPLE (12VIN, 0.85VOUT, IOUT=0A)

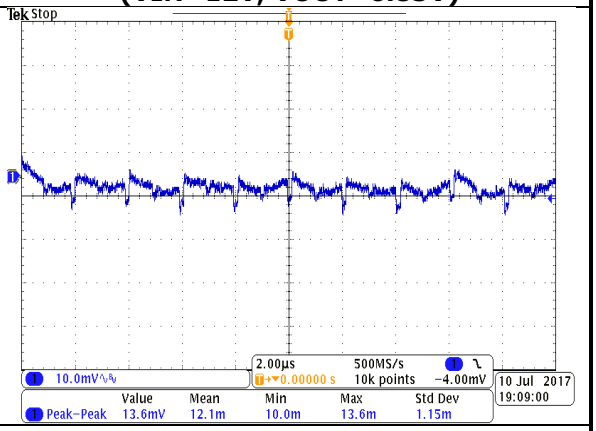


FIG.12 OUTPUT RIPPLE (12VIN, 0.85VOUT, IOUT=60A)

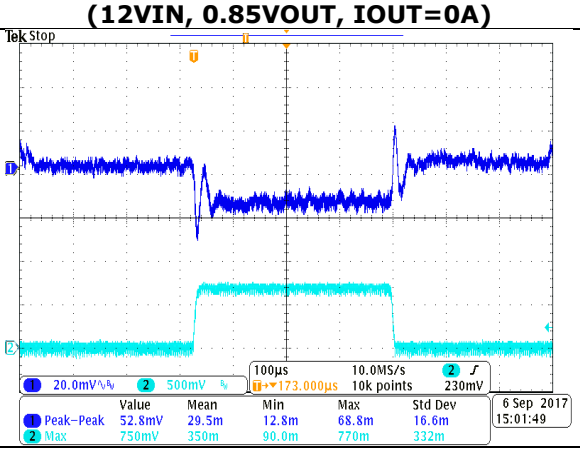


FIG.13 TRANSIENT RESPONSE (12VIN, 0.85VOUT, 0% to 50% LOAD STEP) With Resistor Load 25mΩ

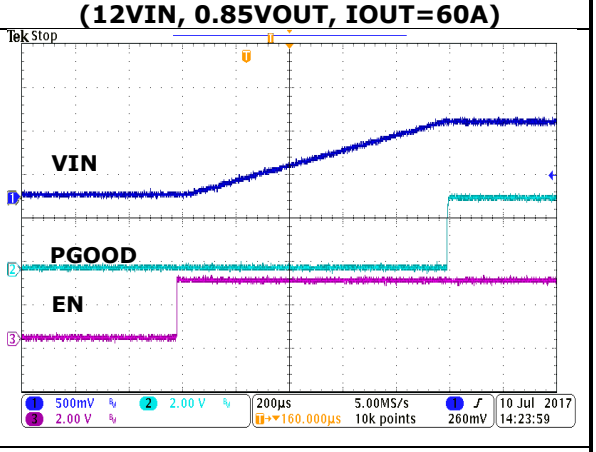


FIG.14 TURN-ON (12VIN, 0.85VOUT, IOUT=0A)

APPLICATION INFORMATION:

REFERENCE CIRCUITFOR GENERAL APPLICATION:

The FIGURE 15 shows the module schematics for input voltage +12V and output voltage +0.85V.

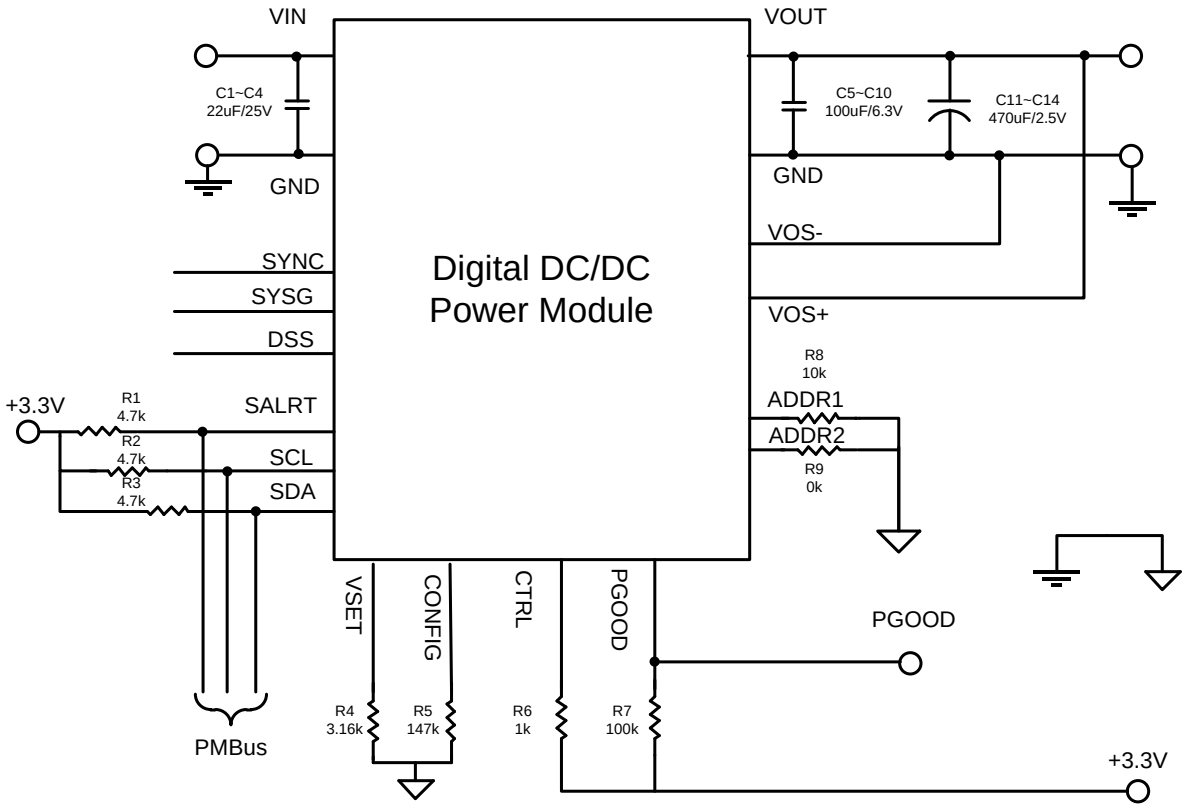


FIGURE.15 TYPICAL APPLICATION FOR POWER MODULE OPERATION

PMBUS LINES AND INPUT

Power Management Bus (PMBus) is implemented over the industry standard SMBus serial interface (a version of I2C) and enables control, programming, and real-time monitoring of compliant products.MSN12AD60-RUD support >50 PMBus commands in addition to several manufacture specific commands related to output voltage, faults, telemetry, and others.

VSET RESISTOR

The MSN12AD60-RUDhas an internal0.6V±0.5% reference voltage. It only programs the dividing resistor R_S which respects to VSET pin and GND. The resistor according to typical output voltage is shown in TABLE 1.

VOUT	0.6V	0.7V	0.75V	0.8V	0.85V	0.9V	0.95V	1.0V	1.05V	1.1V	1.2V	1.5V	1.8V
R_S (kΩ)	0	11.5	18.2	24.9	31.6	38.3	45.3	52.3	59.0	66.5	73.2	80.6	86.6

TABLE 1

The output voltage may also be set to any value between 0.6Vand 1.8V using a PMBus command over the I2C/SMBus interface.

USING CONFIG FOR CONFIGURATION TABLE SELECTION

Using a single resistor RC from CONFIG to SGND, as illustrated in Figure 16, one out of seven configuration tables can be selected in TABLE.2.

Configuration Table Selected	Table #1	Table #2	Table #3	Table #4	Table #5	Table #6	Table #7
R_C (kΩ)	147	133	121	110	100	90.9	82.5
Master/Slave	X	Master	Slave	Slave	Slave	Slave	Slave
Phase Shift	X	X	45°	60°	90°	120°	135°

TABLE 2

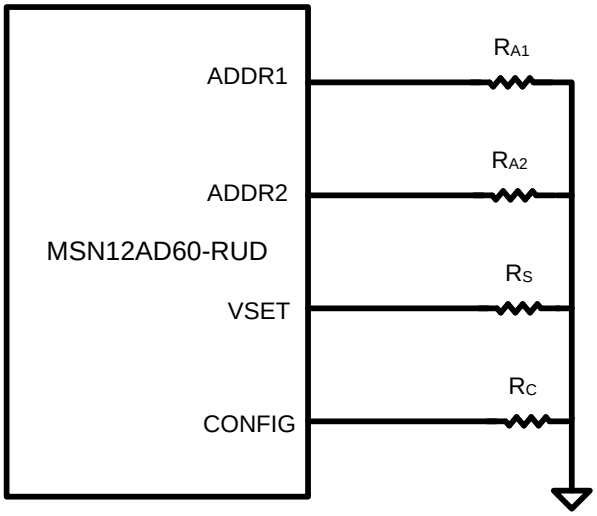


FIGURE.16 Configuration Inputs-VSET

POWER GOOD OUTPUT

The MSN12AD60-RUD provides a power good indicator at its output pin PG. When de-asserted, PG indicates that the output voltage is outside a band around the commanded VOUT set-point. As a consequence PG de-asserts during any serious fault condition where power conversion is stopped. PG auto-clears as soon as the output voltage recovers into the power-good band. When asserted, PG indicates that the output is in regulation, and no major faults present.

The PG output provides a soft internal pull-up resistor (with an approximate value of 54 kΩ) to an internal pull-up voltage (of approximately 2 V).If the PG output is for external purposes, external pull-up resistors with lower and more defined values, connected to a higher pull-up voltage (e.g.,VDD33D) are recommended.

INPUT UVLO

The UVLO ON/OFF thresholds can be set independently using PMBus commands VIN_ON and VIN_OFF. The UVLO fault response is retry. The retry delay is 50 ms. After 50 ms, the controller will check if the under-voltage(UV) condition is still present or not; if not, the module will restart the converter. If the UV condition is still present after the initial 50 ms retry delay, the module will wait an additional 50 ms, and check the status of the fault condition; this process will continue (in 50 ms steps) until the UV condition is no longer present.

INPUT OVLO

The OVLO OFF threshold is set using PMBus command VIN_OV_FAULT_LIMIT. For OVLO a fixed hysteresis of 1 V is applied (assuming standard 20 kΩ / 2kΩ divider on VINSEN). The UVLO fault response is retry. The retry delay is 250 ms. After 250 ms, the module will check if the over-voltage(OV) condition is still present or not; if not, the MSN12AD60-RUD will restart the converter. If the OV condition is still present after the initial 250 ms retry delay, the controller will wait an additional 50 ms, and check the status of the fault condition; this process will continue (in 50 ms steps) until the OV condition is no longer present.

CONFIGURATION INPUT ADDR1 AND ADDR2

Configuration inputs ADDR1 and ADDR2 in conjunction with resistors RA1 and RA2 are used to assign a PMBus address to a MSN12AD60-RUD. Unique MSN12AD60-RUD addresses are required in systems where multiple PMBus MSN12AD60-RUDs are connected to a single serial synchronous bus, through lines SDA (data) and SCL (clock). Bus conflicts will occur if more than one MSN12AD60-RUD responds to the same PMBus address (other than the broadcast address). It is up to the system architect to ensure that unique PMBus addresses are applied to communication MSN12AD60-RUDs. PMBus addresses lower than 16 and higher than 119 should be avoided as they are reserved for special communication purposes. Table 3 offers a summary of assigned PMBus address versus configuration resistors RA1 and RA2.

If serial communication is not required, or the factory-default PMBus address of 16 decimal is agreeable, or MSN12AD60-RUD parts with a customer-specific MSN12AD60-RUD address have been ordered, inputs ADDR1 and ADDR2 may be left floating.

PMBus addresses below 16 cannot be selected through configuration inputs ADDR1 and ADDR2 as this range is set aside for specific protocols (such as Alert Response, Broadcast, etc.). Should an address in that range be required for specific purposes, it can be assigned through serial communication, customer-specific part configuration, or through flexible configuration input CONFIG.

		Resistor RA2							
		0kΩ	10.0kΩ	13.3kΩ	17.8kΩ	21.5kΩ	26.1kΩ	31.6kΩ	∞
Resistor RA1	0kΩ	16	32	48	64	80	96	112	16
	10.0kΩ	17	33	49	65	81	97	113	17
	13.3kΩ	18	34	50	66	82	98	114	18
	17.8kΩ	19	35	51	67	83	99	115	19
	21.5kΩ	20	36	52	68	84	100	116	20
	26.1kΩ	21	37	53	69	85	101	117	21
	31.6kΩ	22	38	54	70	86	102	118	22
	34.8kΩ	23	39	55	71	87	103	119	23
	38.3kΩ	24	40	56	72	88	104	-	24
	42.2kΩ	25	41	57	73	89	105	-	25
	46.4kΩ	26	42	58	74	90	106	-	26
	51.1kΩ	27	43	59	75	91	107	-	27
	56.2kΩ	28	44	60	76	92	108	-	28
	61.9kΩ	29	45	61	77	93	109	-	29
	68.1kΩ	30	46	62	78	94	110	-	30
	75.0kΩ	31	47	63	79	95	111	-	31
	82.5kΩ	32	48	64	80	96	112	16	32
	90.9kΩ	33	49	65	81	97	113	16	33
	100kΩ	34	50	66	82	98	114	16	34
	110kΩ	35	51	67	83	99	115	16	35
	121kΩ	36	52	68	84	100	116	16	36
	133kΩ	37	53	69	85	101	117	16	37
	147kΩ	38	54	70	86	102	118	16	38
	∞	39	55	71	87	103	119	16	16

TABLE 3 PMBus Address Configuration through Configuration Resistors RA1 and RA2

CONTROL INPUT (CTRL)

The MSN12AD60-RUD provides a PMBus compliant power conversion control signal through input CTRL. Input CTRL can be configured through standard PMBus command ON_OFF_CONFIG.

The control pin can be configured to be ignored, in which case power conversion is enabled as soon as all other conditions are satisfied (i.e., power conversion activated through PMBus OPERATION command if not ignored, and no faults preventing power conversion).

If CTRL is configured not to be ignored, its polarity can be set to active high or active low. If CTRL is configured "Active High", the CTRL pin must be pulled above the VIH input threshold in order to commence power conversion. If CTRL is configured "Active Low", the CTRL pin must be pulled below VIL in order to enable power conversion.

In compliance with the PMBus specification, the CTRL pin does not sink or source any leakage currents (and hence does not provide any internal pull-up or pull-down resistors). External components must be used in order to ensure that CTRL is always driven to the desired logic level.

Programmable Load-Line

This controller supports a programmable load-line function to reduce the peak-to-peak deviation in output voltage during transient events. The load-line function adjusts the set-point as a function of output current according to the formula:

$V_{OUT} = V_{SET} - (I_{OUT} \times R_{LL})$

where RLL is the effective resistance of the load line. This is shown conceptually in Figure 17 RLL is adjustable from 0 mΩ to greater than 20 mΩ (typical), with the upper limit depending upon application-specific parameters. The default value is 0 mΩ, and the minimum increment is less than 0.1 mΩ.

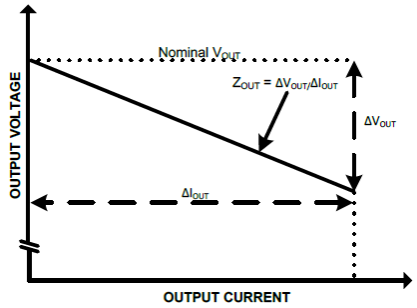


FIGURE.17 VOUT vs. IOUT with Load-Line Enabled

Additionally, a programmable low-pass filter is provided to allow optimization of the dynamic response. The pole frequency, FP, is adjustable from below 1 kHz to greater than20 kHz (typical), with the precise range depending upon application-specific parameters. The default value for pole frequency is 10 kHz, and the minimum increment is less than100 Hz. MSN12AD60-RUD's load-line implementation is illustrated in Figure 18.

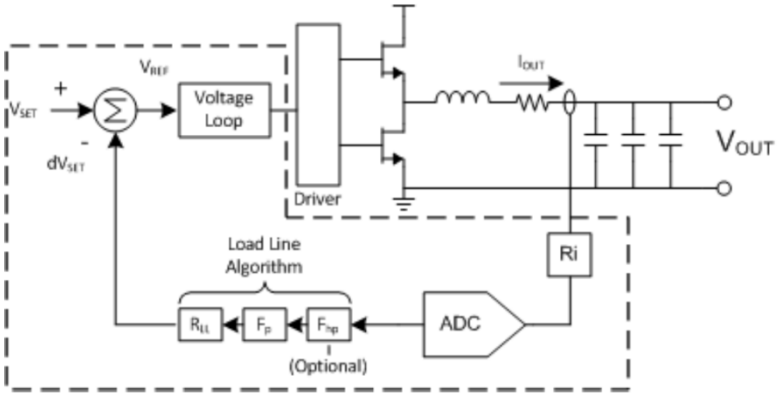


FIGURE.18 Load-Line Implementation

Output Overvoltage Protection (OVP)

The MSN12AD60-RUD provides OVP functionality through pins VSENP and VSENN. The OVP threshold can be set through command BVOUT_OV_FAULT_LIMIT (in addition to any other alternative configuration method).

The OVP fault response can be configured as latching or retry. When using the latching feature, the input voltage is cycled to clear the latch. When using the retry feature, the retry delay (relaxation period) is 2000 ms. After 2000 ms, the MSN12AD60-RUD will attempt to restart the converter. The response delay to an OVP event is programmable. During the design phase, users may program the OVP response delay by using the PowerSMART GUI-based design tool. The MSN12AD60-RUD provides an OVP event counter that is used to determine how quickly the MSN12AD60-RUD responds to OV conditions. This counter (N) is up/down counter that can be configured to enable the MSN12AD60-RUD's OV fault protection.

OVER-CURRENT PROTECTION (OCP)

The OCP threshold can be set through command IOUT_OC_FAULT_LIMIT (in addition to any other alternative configuration method). The OCP fault response can be configured as latching or retry. When using the latching feature, the input voltage is cycled, or ON/OFF toggled, to clear the latch. When using the retry feature, the retry delay is programmable from 1 ms to 65,535ms in 1 ms steps. After reaching the programmed retry delay, the MSN12AD60-RUD will attempt to restart the converter.

SHORT-CIRCUIT PROTECTION (SCP)

Short-circuit protection (analog) provides a fast, temperature compensated over-current protection mechanism for ultra-fast response to severe and instantaneous over-current conditions (e.g., output short-circuits). It should be noted that in order to minimize response delay, SCP is based on the gained current sense signal prior to quantization and temperature correction.

The SCP fault can be configured as latching or retry. When using the latching feature, the input voltage is cycled, or ON/OFF toggled, to clear the latch. The retry delay is fixed at 500 ms. After reaching the retry delay, the MSN12AD60-RUD will attempt to restart the converter.

With this scheme SCP response delay of 400 ns are achievable. Hence, SCP will provide coarse but low-latency protection, while the MSN12AD60-RUD's OCP block (digital) provides more precisely defined threshold, but not with the response delay of the SCP block. The SCP threshold is set through amanufacturer-specific command as there is no SCP mechanism defined in the PMBus protocol.

OVER TEMPERATURE PROTECTION (OTP)

Over-temperature protection is supported in order to protect the power conversion system, its components, and the load it supplies. The OTP threshold can be configured using any configuration method (i.e., factory-default or customer specific part configuration, CONFIG pin-programming, PMBus communication through the standard command OT_FAULT_LIMIT). The OTP fault can be configured as latching or retry. When using the latching feature, the input voltage is cycled, or ON/OFF toggled, to clear the latch. The retry delay is 500 ms, and uses a fixed hysteresis of 15°C. After 500 ms, the controller will check if the over-temperature (OT) condition is still present or not; if not, the MSN12AD60-RUD will restart the converter. If the OT condition is still present after the initial 500 ms retry delay, the controller will wait an additional 50ms, and check the status of the fault condition; this process will continue (in 50 ms steps) until the OT condition is no longer present.

DIGITAL STRESS SHARE (DSS) SINGLE WIRE BUS

MSN12AD60-RUD can be connected in parallel for higher phase, higher current outputs. A single wire, digital interface called DSS facilitates current sharing between the regulators. The proprietary current sharing architecture forms an outer current feedback loop which can be tuned for performance via several parameters. Referring to Figure 2, the input to the current loop is the average of all regulator currents (total output current). The average is estimated as the median of the minimum and maximum currents over all regulators on the DSS bus. This method is considered democratic as every regulator contributes its current information to the DSS bus. It also ensures that the current loop bandwidth is not compromised by adding more regulators to the bus (since only minimum and maximum currents are sampled).

The current loop in each controller has a proportional compensator with adjustable gain (DSS BW) and saturation thresholds. From a small signal analysis prospective, the proportional compensator provides good transient performance, and does not reduce the phase response vs. frequency, as an integral compensator would. However, there will be a steady state offset error as the DC gain is finite(this error is in terms of current matching offsets). To correct for the offset error, an auto-zero (AZ) term is introduced. The AZ block provides excellent current matching accuracy without the small signal disadvantages of an integrator. As the AZ block adds an offset into the current loop, one regulator in the DSS system must have the AZ block disabled to maintain the absolute reference for accurate voltage regulation. Disabling the AZ block will result in a slight off set in current matching for the affected regulator, however this is quite small and bounded by the matching of the other regulators on the DSS bus. Typical current matching accuracy is with +/- 1 A.

SYNCHRONIZATION

All regulators participating in parallel regulation should have synchronized and offset switching frequencies to avoid beat frequencies and to lower RMS current ripple on the input and output. This is easily accomplished by connecting all the SYNC pins together, and configuring each controller appropriately. There are two ways to configure synchronization.

The first is that one controller can be set as a master clock source and will output a clock signal from the SYNC pin, while the other controllers are set as slaves. This method employs a phase lock loop to synchronize to the clock signal and maintain a programmable phase offset.

The second method to achieve synchronization is to provide a master clock from the system and configure all the controllers to be slaves with specified offsets. When programming the phase offset, keep in mind that for two-phase controllers, the two phases within this controller are always 180° apart. For example, in a 4 phase system using 2 two-phase controllers, one controller is set at 0° offset and the other is set at 90° to achieve an equal phase distribution (i.e., 0°, 90°, 180°, and 270°). See Synchronization Line (SYNC) section for more information.

SYSTEM GOOD FLAGS

The SYSG pins can be connected together to achieve synchronized fault sharing. This is an important feature in a parallel connected system, as a fault in one controller should be viewed as a fault for all the controllers. In addition, tying SYSG together ensures that all phases respond to the fault in unison. See the System Good Line (SYSG) section for more information.

PHASE CURRENT SHARING

The temperature-corrected quantized phase currents are communicated to other controllers through module proprietary single-wire DSS bus, so that multiple participating MSN12AD60-RUD in a system can share the total load current.

REFLOW PARAMETERS:

Lead-free soldering process is a standard of electronic products production. Solder alloys like Sn/Ag, Sn/Ag/Cu and Sn/Ag/Bi are used extensively to replace the traditional Sn/Pb alloy. Sn/Ag/Cu alloy (SAC) is recommended for this power module process. In the SAC alloy series, SAC305 is a very popular solder alloy containing 3% Ag and 0.5% Cu and easy to obtain. Figure 19 shows an example of the reflow profile diagram. Typically, the profile has three stages. During the initial stage from room temperature to 150°C, the ramp rate of temperature should not be more than 3°C/sec. The soak zone then occurs from 150°C to 200°C and should last for 60 to 120 seconds. Finally, keep at over 217°C for 60 seconds limit to melt the solder and make the peak temperature at the range from 240°C to 250°C. It is noted that the time of peak temperature should depend on the mass of the PCB board. The reflow profile is usually supported by the solder vendor and one should adopt it for optimization according to various solder type and various manufacturers' formulae.

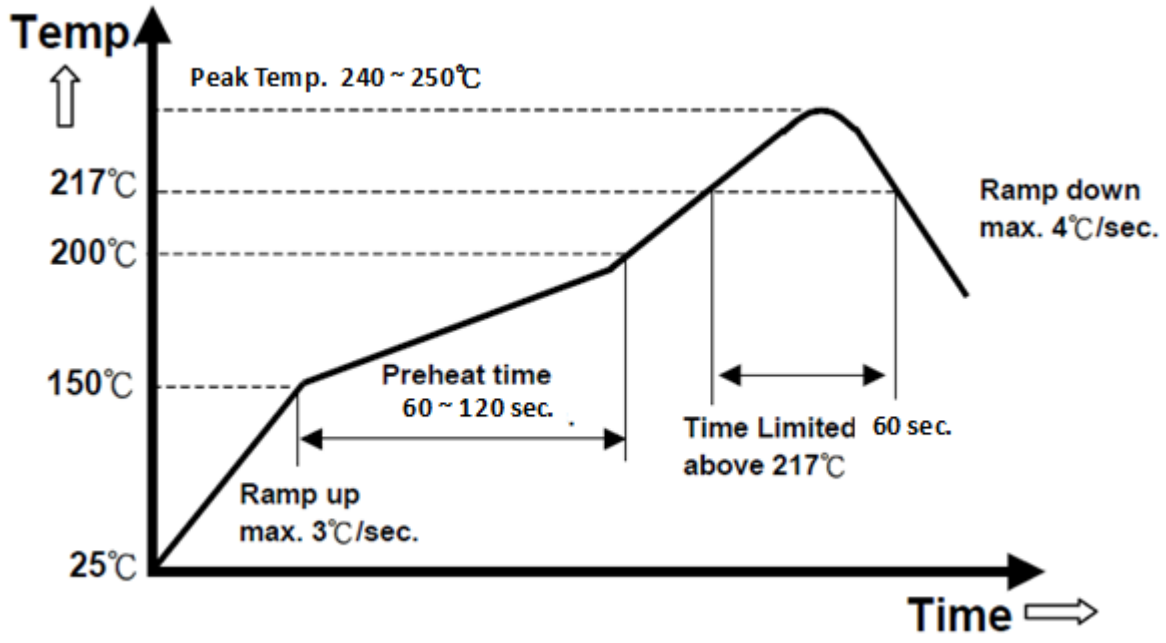
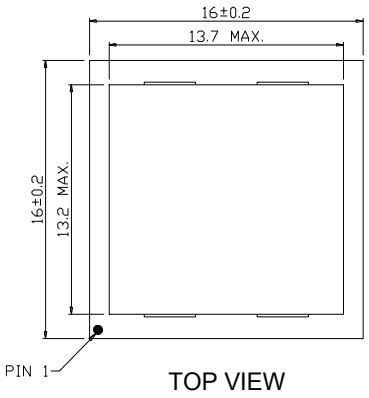
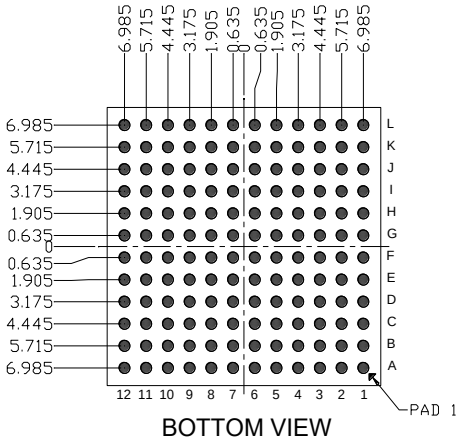


FIG.19 Recommendation Reflow Profile

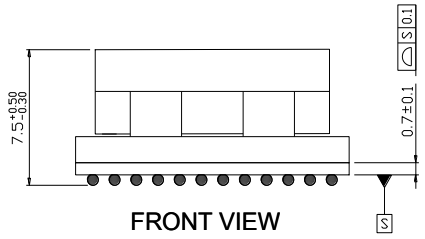
PACKAGE OUTLINE DRAWING:



TOP VIEW



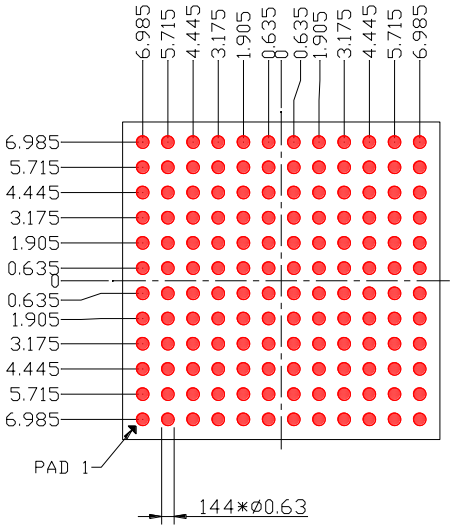
BOTTOM VIEW



FRONT VIEW

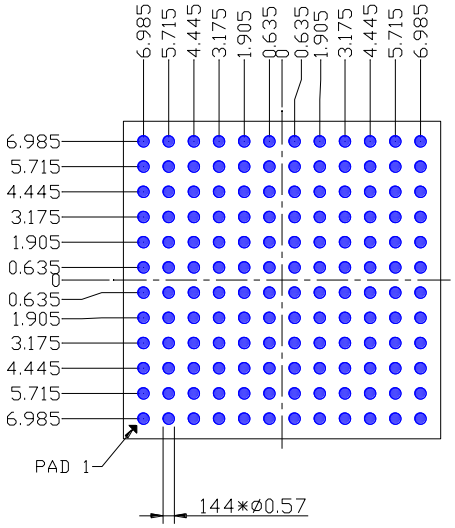
*All dimensions in mm
*Tolerance: X.X±0.2
X.XX±0.15
X.XXX±0.10

LAND PATTERN REFERENCE:



Unit: mm
General Tolerances:±0.2mm

TOP VIEW
TYPICAL RECOMMENDED LAND PATTERN



Unit: mm
General Tolerances:±0.2mm

TOP VIEW
STENCIL PATTERN WITH SQUARE PADS

REVERSION HISTORY:

Date	Revision	Changes
2017.07.10	00	Release the preliminary specification.
2017.09.26	01	Change P/N from MMF12AD60-RUD to MSN12AD60-RUD. Change POD pin define. Add pin 1 index in pin configuration and POD. Add PMBUS commands in appendix.
201712.01	02	Add config table for selection master and slave phase shift. Add reflow parameters.

APPENDIX A: STANDARD PMBUS COMMANDS

Command	Code(hex)	R/W	#Bytes	Coefficients(Decimal)
OPERATION	01	R/W	1	N/A
ON_OFF_CONFIG	02	R/W	1	N/A
CLEAR_FAULTS	03	-	0	N/A
STORE_DEFAULT_ALL	11	-	0	N/A
RESTORE_DEFAULT_ALL	12	-	0	N/A
VOUT_MODE	20	R	1	N/A
VOUT_COMMAND	21	R/W	2	m = 5120, R = b = 0
VOUT_TRIM	22	R/W	2	m = 5120, R = b = 0
VOUT_MAX	24	R/W	2	m = 5120, R = b = 0
VOUT_MARGIN_HIGH	25	R/W	2	m = 5120, R = b = 0
VOUT_MARGIN_LOW	26	R/W	2	m = 5120, R = b = 0
VOUT_TRANSITION_RATE	27	R/W	2	m = 256, R = b = 0
VOUT_SCALE_LOOP	29	R/W	2	m = 16384, R = b = 0
VOUT_SCALE_MONITOR	2A	R	2	m = 16384, R = b = 0
FREQUENCY_SWITCH	33	R/W	2	m = 1, R = b = 0
VIN_ON	35	R/W	2	m = 1862, R = b = 0 (See †)
VIN_OFF	36	R/W	2	m = 1862, R = b = 0 (See †)
INTERLEAVE	37	R/W	2	N/A
IOUT_CAL_GAIN	38	R/W	2	m = 512, R = b = 0
IOUT_CAL_OFFSET	39	R/W	2	m = 10.24, R = b = 0
VOUT_OV_FAULT_LIMIT	40	R/W	2	m = 5120, R = b = 0
VOUT_UV_FAULT_LIMIT	44	R/W	2	m = 5120, R = b = 0
IOUT_OC_FAULT_LIMIT	46	R/W	2	m = 10.24, R = b = 0
OT_FAULT_LIMIT	4f	R/W	2	m = 1, R = b = 0
OT_WARN_LIMIT	51	R/W	2	m = 1, R = b = 0
UT_WARN_LIMIT	52	R/W	2	m = 1, R = b = 0
UT_FAULT_LIMIT	53	R/W	2	m = 1, R = b = 0
VIN_OV_FAULT_LIMIT	55	R/W	2	m = 1862, R = b = 0 (See †)
TON_DELAY	60	R/W	2	m = 62.56, R = b = 0
TON_RISE	61	R/W	2	m = 32, R = b = 0
TOFF_DELAY	64	R/W	2	m = 62.56, R = b = 0
STATUS_BYTE	78	R	1	N/A
STATUS_WORD	79	R	2	N/A
STATUS_VOUT	7a	R	1	N/A
STATUS_IOUT	7b	R	1	N/A
STATUS_INPUT	7c	R	1	N/A
STATUS_TEMPERATURE	7d	R	1	N/A
STATUS_CML	7e	R	1	N/A
READ_EOUT	87	R	7	(See ††)
READ_VIN	88	R	2	m = 1862, R = b = 0 (See †)
READ_VOUT	8b	R	2	m = 640, R = b = 0
READ_IOUT	8c	R	2	m = 10.24, R = b = 0

APPENDIX A: STANDARD PMBUS COMMANDS

Command	Code(hex)	R/W	#Bytes	Coefficients(Decimal)
READ_TEMPERATURE_1	8d	R	2	m = 1, R = b = 0
READ_TEMPERATURE_2	8e	R	2	m = 1, R = b = 0
READ_TEMPERATURE_3	8f	R	2	m = 1, R = b = 0
READ_DUTY_CYCLE	94	R	2	m = 10, R = b = 0
READ_FREQUENCY	95	R	2	m = 32, R = b = 0
PMBUS_REVISION	98	R	1	N/A
MFR_ID	99	R	17	N/A
MFR_MODEL	9a	R	17	N/A
MFR_REVISION	9b	R	17	N/A
MFR_LOCATION	9c	R	17	N/A
MFR_DATE	9d	R	17	N/A
MFR_SERIAL	9e	R	17	N/A