Cyntec Power Module Solutions for FPGA
MUN12AD05-SMFL

Cyntec Co., Ltd.

Smarter & Greener
**FEATURES:**
- High Density uPOL Module
- 5A Output Current
- Input Voltage Range from 4.5 to 20V
- Output Voltage Range
  - 1.9V to 5V for MUN12AD05-SMFH
  - 0.6V to 1.8V for MUN12AD05-SMFL
- 92% Peak Efficiency (@Vin=12V)
- Enable / PGOOD Function
- Force PWM Mode
- Protections (Non-latching: OCP, OTP, SCP, OVP)
- Internal Soft Start
- Compact Size: 6mm*6mm*3.5mm (Max)
- Pb-free for RoHS compliant
- MSL 2, 250°C Reflow

**APPLICATIONS:**
- Distributed Power Supply
- Server, Workstation, and Storage
- Networking and Datacom
Specifications
**VCCAUX/VCCAUX_IO/VCCADC**
- 1.8V, current 0.5~4A, additional current may be needed for IO
- Transient response: ±3%, 90% step, 10A/us
- Decoupling capacitance: 4x47uF
MUN12AD05-SMFL for Xilinx XCVU13P

**Efficiency**

**Test Condition**

VIN=5V, 12V, 20V, VOUT=1.8V, IOUT=5A

Module: Cyntec MUN12AD05-SMFL X 1pcs

Input Capacitor: 10uF x 1pcs

Output Capacitor: 47uF x 4pcs

VIN=12V VOUT=1.8V Pk-Pk Efficiency=87% for IOUT=4A
MUN12AD05-SMFL for Xilinx XCVU13P

Ripple

Test Condition
VIN=12V, VOUT=1.8V, IOUT=5A
Module: Cyntec MUN12AD05-SMFL X 1pcs
Input Capacitor: 10uF x 1pcs
Output Capacitor: 47uF x 4pcs

VOUT=1.8V Pk-Pk 5.28 mV for IOUT=5 A
Test Condition
VIN=12V VOUT=1.8V IOUT=0~3.6A
Module: Cyntec MUN12AD05-SMFL X 1pcs
Input Capacitor: 10uF x 1pcs
Output Capacitor: 47uF x 4 pcs
Transient < ±3%, >90% step, 10A/us with output

\[ \text{VOUT}=1.8V \text{ Pk-Pk Transient} = 93.2mV \text{ for IOUT}=0\sim3.6A \]
MUN12AD05-SMFL for Xilinx XCVU13P
Thermal

Test Condition
VIN=12V VOUT=1.8V IOUT=5A
Module: Cyntec MUN12AD05-SMFL X 1 pcs
Input Capacitor: 10uF x 1pcs
Output Capacitor: 47uF x 4pcs

MUN12AD05-SMFL De-rating

0 LMF 81℃ De-rating
Layout Example of the 5A module
(Layout is for reference only --- single-sided SMT. Further optimization is possible in terms of output characteristics and actual application environment)

Remarks
• Input capacitance: 10uF
• Output capacitance: 47uF x 4pcs
• Arrangement could be optimized based on output transient requirements